Click here for production status of specific part numbers.

MAX20004/MAX20006/ MAX20008

36V, 220kHz to 2.2MHz, 4A/6A/8A Fully Integrated Automotive Step-Down Converters

General Description

The MAX20004/MAX20006/MAX20008 are small, synchronous, automotive buck converter devices with integrated high-side and low-side MOSFETs. The device family can deliver up to 8A with input voltages from 3.5V to 36V, while using only 25µA quiescent current at no load. Voltage quality can be monitored by observing the $\overline{\text{RESET}}$ signal. The devices can operate in dropout by running at 98% duty cycle, making them ideal for automotive applications.

The devices offer fixed output voltages of 5V and 3.3V, along with the ability to program the output voltage between 1V and 10V. Frequency is resistor programmable from 220kHz to 2.2MHz. The devices offer a forced fixed-frequency PWM mode (FPWM) and skip mode with ultra-low quiescent current. The devices can be factory programmed to enable spread-spectrum switching to reduce EMI.

The MAX20004/MAX20006/MAX20008 are available in a small, 3.5mm x 3.75mm, 17-pin FC2QFN package and use very few external components.

Applications

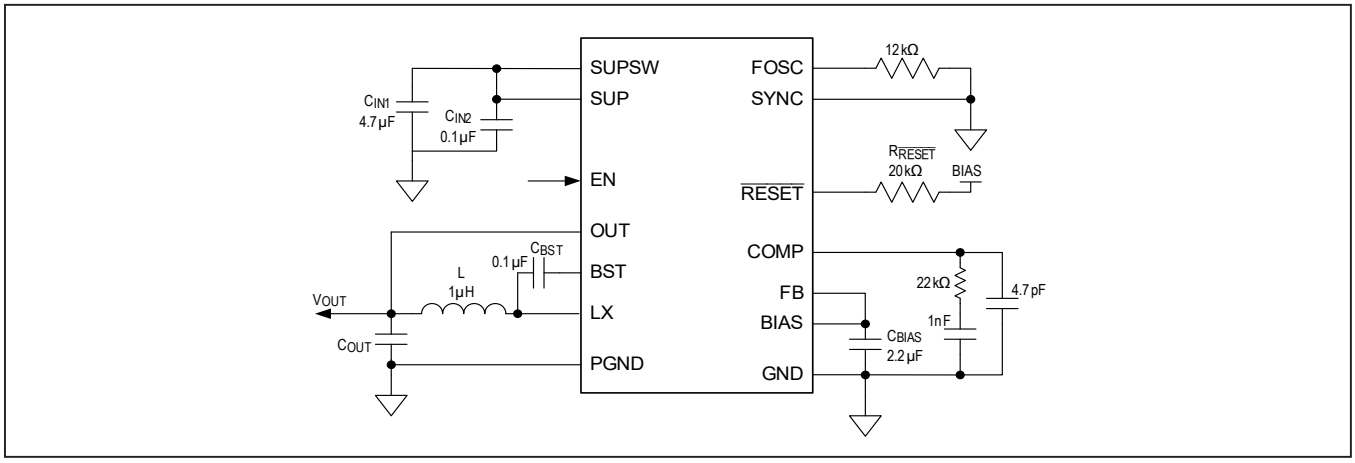
- Point-of-Load (PoL) Applications in Automotive
- Distributed DC Power Systems
- Navigation and Radio Head Units

Benefits and Features

- Multiple Functions for Small Size
  - Operating V_{IN} Range of 3.5V to 36V
  - 25µA Quiescent Current in Skip Mode
  - Synchronous DC-DC Converter with Integrated FETs
  - 220kHz to 2.2MHz Adjustable Frequency
  - Fixed 5ms Internal Soft-Start
  - Programmable 1V to 10V Output, or 3.3V and 5.0V Fixed-Output Options Available
  - 98% Duty-Cycle Operation with Low Dropout
  - $\overline{\text{RESET}}$ Output
- High Precision
  - ±2% Output-Voltage Accuracy
  - Good Load-Transient Performance
- Robust for the Automotive Environment
  - Current-Mode, Forced-PWM and Skip Operation
  - Overtemperature and Short-Circuit Protection
  - 3.5mm x 3.75mm 17-Pin FC2QFN
  - -40°C to +125°C Operating Temperature Range
  - 40V Load-Dump Tolerant
  - AEC-Q100 Qualified

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



maxim integrated™

Absolute Maximum Ratings

SUP, EN, SUPSW to PGND ..... -0.3V to +40V
LX to PGND (Note 1) ..... -0.3V to (V_{SUPSW} + 0.3V)
BIAS, $\overline{RESET}$ to GND ..... -0.3V to +6.0V
FOSC, COMP to GND ..... -0.3V to (V_{BIAS} + 0.3V)
SYNC, FB to GND ..... -0.3V to (V_{BIAS} + 0.3V)
GND to PGND ..... -0.3V to +0.3V
OUT to PGND ..... -0.3V to +12V
BST to LX ..... -0.3V to +6V
LX Continuous RMS Current 8A
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
17-Pin FC2QFN (derate 29.4mW/°C > 70°C) 2553mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Package Information

17 FC2QFN

Package Code	F173A3FY+1
Outline Number	21-100155
Land Pattern Number	90-100056
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	27°C/W
Junction to Case (θ_{JC})	2.6°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the EV kit. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{SUP} = V_{SUPSW} = V_{EN} = 14V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}, V_{SUPSW}			3.5		36	V
Supply Voltage Range	V_{SUP}, V_{SUPSW}	After startup		3.0			V
Supply Current	I_{SUP}	Skip mode, no load	V_{OUT} = 3.3V		25	32	µA
			V_{OUT} = 5.0V		30	42	
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V			5	10	µA
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = V_{SUPSW} = 6V to 40V I_{BIAS} < 10mA, BIAS not switched over to V_{OUT}			5		V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} rising		2.7	3	3.3	V

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW} = V_{EN} = 14V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} falling		2.5	2.9	V
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising		175		°C
Thermal-Shutdown Hysteresis	T_{HYST}			15		°C
OUTPUT VOLTAGE						
PWM-Mode Output Voltage (Note 3)	V_{OUT_5V}	V_{SUP} = V_{SUPSW} = 6V to 28V	4.9	5	5.1	V
Skip-Mode Output Voltage (Note 4)	V_{SKIP_5V}	Skip mode, no load, FB = BIAS	4.9	5	5.15	V
PWM-Mode Output Voltage	$V_{OUT\_3.3V}$	V_{SUP} = V_{SUPSW} = 6V to 28V	3.23	3.3	3.37	V
Skip-Mode Output Voltage (Note 4)	$V_{SKIP\_3.3V}$	Skip mode, no load, FB = BIAS	3.23	3.3	3.4	V
Load Regulation	LN_{REG}	V_{FB} = V_{BIAS}, 30mA < I_{LOAD} < 6A, PWM mode, 5V		0.6		%
Line Regulation	LD_{REG}	V_{FB} = V_{BIAS}, 6V < V_{SUPSW} < 36V, PWM mode		0.02		%/V
BST Input Current	I_{BST_ON}	High-side MOSFET on, V_{BST} - V_{LX} = 5V		1.5		mA
BST Input Current	IBST_OFF	High-side MOSFET off, V_{BST} - V_{LX} = 5V		0.1		µA
LX Current Limit	I_{LX}	MAX20004 (4A)	5.25	7	8.75	A
		MAX20006 (6A)	7.5	10	12.5	
		MAX20008 (8A)	10.5	14	17.5	
LX Rise Time (Note 4)	t_{LX_TR}			2		ns
Spread Spectrum	SS	Spread spectrum enabled		±3		%
High-Side Switch On-Resistance	R_{HS}	V_{BIAS} = 5V, I_{LX} = 2A		38	76	mΩ
High-Side Switch Leakage	I_{HS_LKG}	High-side MOSFET off, V_{SUPSW} = 36V, V_{LX} = 0V, T_A = +25°C		1	5	µA
Low-Side Switch On-Resistance	R_{LS}	V_{BIAS} = 5V, I_{LX} = 2A		18	36	mΩ
Low-Side Switch Leakage	I_{LS_LKG}	Low-side MOSFET off, V_{SUPSW} = 36V, V_{LX} = 36V, T_A = +25°C		1	5	µA
FB Input Current	I_{FB}	T_A = +25°C		30	100	nA
FB Regulation Voltage	V_{FB}	FB connected to an external resistive divider, 6V < V_{SUPSW} < 36V	0.99	1.00	1.01	V
Transconductance (from FB to COMP)	g_m	V_{FB} = 1V, V_{BIAS} = 5V	500	780	1000	µS
Minimum On-Time (Note 4)	t_{ON_MIN}	Load 500mA (Note 4)		75		ns

Electrical Characteristics (continued)

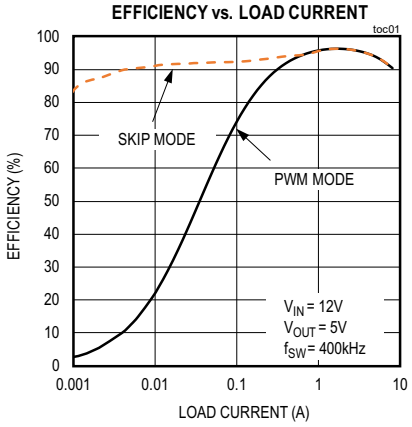
(V_{SUP} = V_{SUPSW} = V_{EN} = 14V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

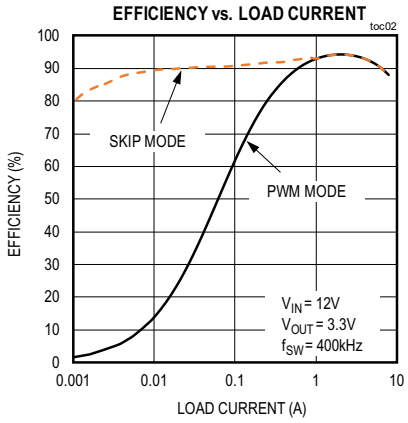
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Duty Cycle	DC_{MAX}		97	98		%
Oscillator Frequency	f_{SW1}	R_{FOSC} = 73.2kΩ	360	400	440	kHz
Oscillator Frequency	f_{SW2}	R_{FOSC} = 12kΩ	2.0	2.2	2.4	MHz
Soft-Start Time	t_{SS}			5		ms
EN, SYNC						
External Input Clock Frequency		R_{FOSC} = 12kΩ (Note 5)	1.8		2.6	MHz
SYNC High Threshold	V_{SYNC_HI}		1.4			V
SYNC Low Threshold	V_{SYNC_LO}				0.4	V
SYNC Leakage Current	I_{SYNC}	T_A = +25°C		0.1	1	µA
EN High Threshold	V_{EN_HI}		2.4			V
EN Low Threshold	V_{EN_LO}				0.6	V
EN Hysteresis	V_{EN_HYS}			0.2		V
EN Leakage Current	I_{EN}	T_A = +25°C		0.1	2	µA
$\overline{\text{RESET}}$						
UV Threshold	UV_{ACC}	Falling	89	91	93	%
UV Hysteresis				3		%
Hold Time (Note 6)	t_{HOLD1}	(Note 6)		0.2		ms
UV Debounce Time	t_{DEB}			25		µs
OV Protection Threshold	OVP_{THR}	Rising	104	107	110	%
OV Protection Threshold	OVP_{THF}	Falling		105		%
Leakage Current	I_{RST_LKG}	V_{OUT} in regulation, T_A = +25°C			1	µA
Output Low Level	V_{ROL}	I_{SINK} = 5mA			0.4	V

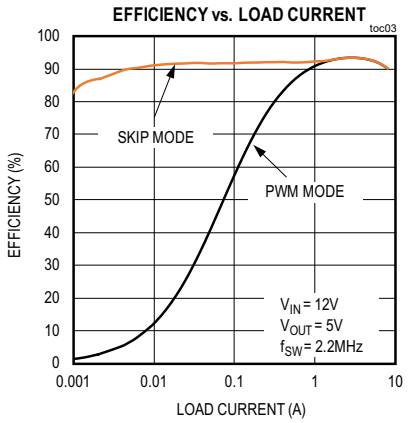
Note 2: All units are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: Device not in dropout condition.
Note 4: Guaranteed by design. Not production tested.
Note 5: Contact factory for SYNC frequency outside the specified range.
Note 6: Contact factory for additional options.

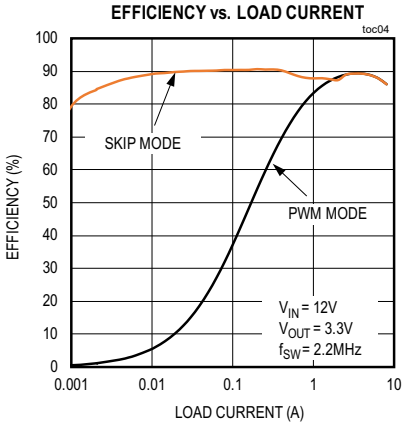
Typical Operating Characteristics

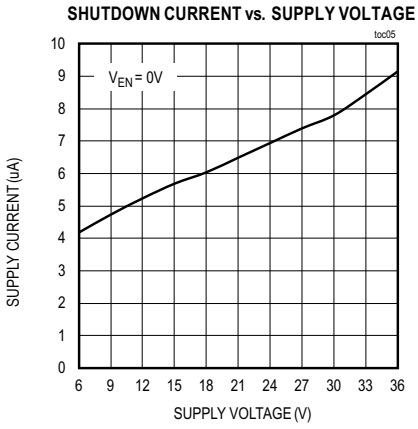
(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FSYNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

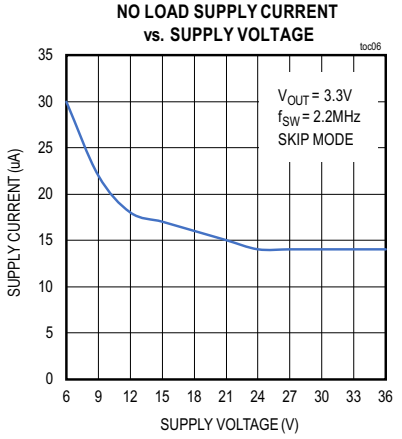








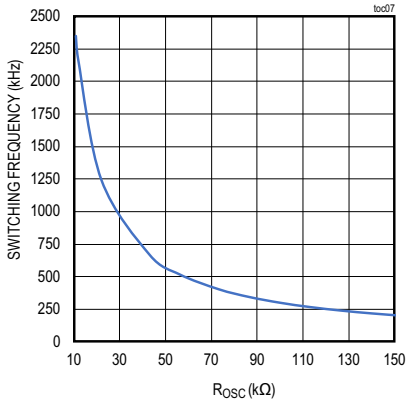




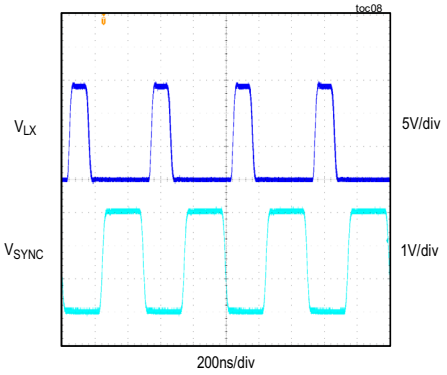
Typical Operating Characteristics

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FSYNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

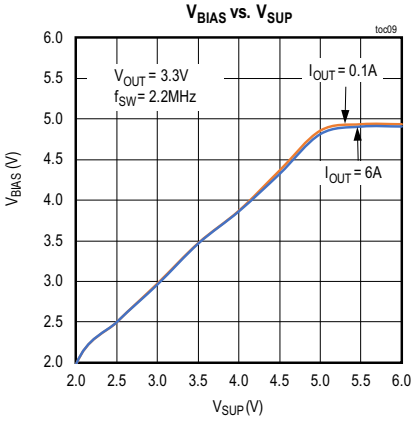
SWITCHING FREQUENCY vs. R_{FOSC}



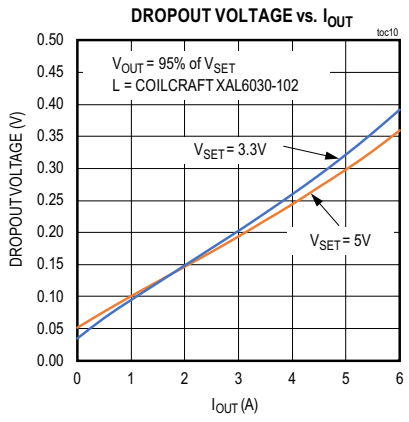
SYNC FUNCTION



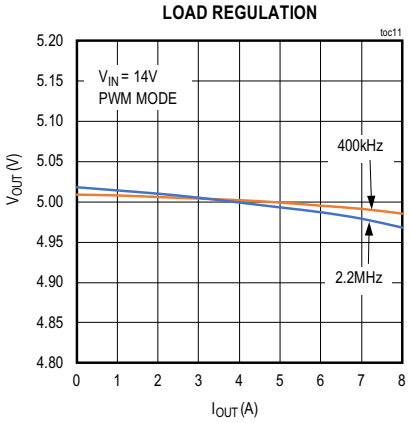
V_{BIAS} vs. V_{SUP}



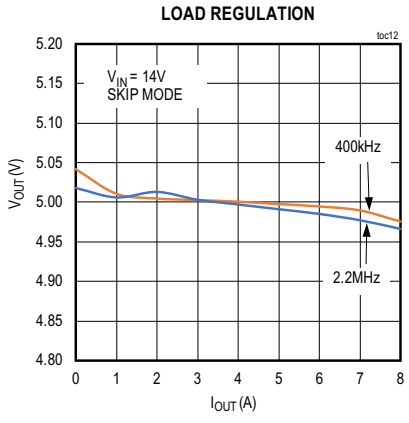
DROPOUT VOLTAGE vs. I_{OUT}



LOAD REGULATION



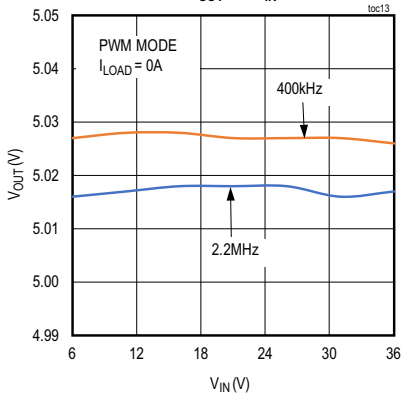
LOAD REGULATION



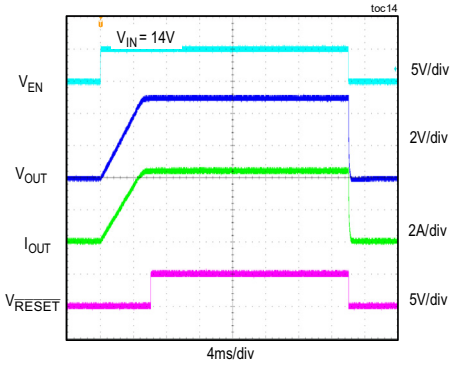
Typical Operating Characteristics

(V_{SUP} = V_{SUPSW} = 14V, V_{EN} = 14V, V_{OUT} = 5V, V_{FSYNC} = 0V, R_{FOSC} = 12kΩ, T_A = +25°C, unless otherwise noted.)

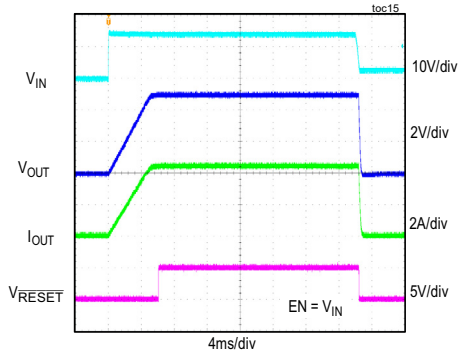
V_{OUT} vs. V_{IN}



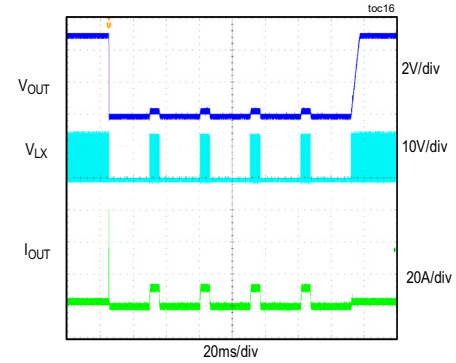
ENABLE STARTUP BEHAVIOR



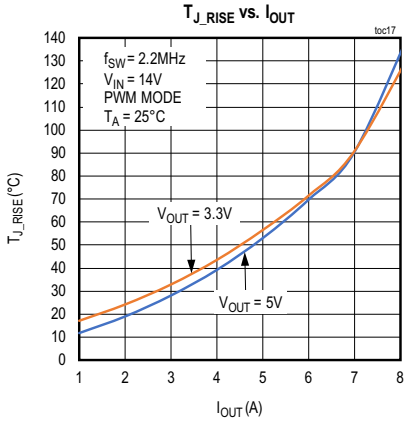
V_{IN} STARTUP BEHAVIOR



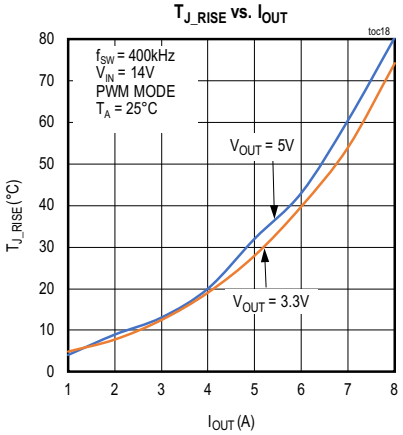
SHORT CIRCUIT AND RECOVERY



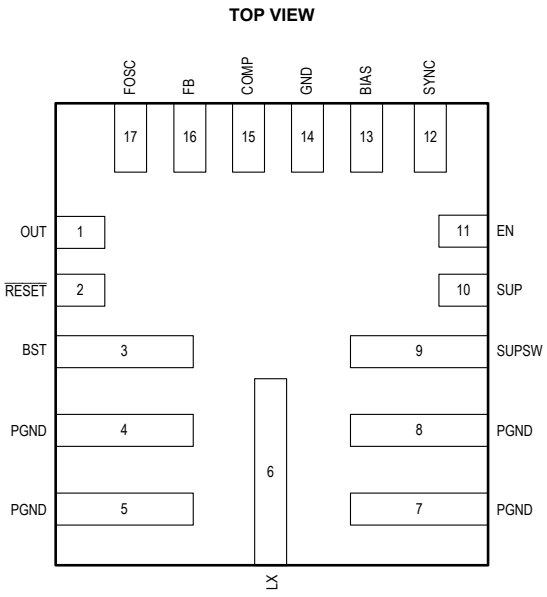
T_{J_RISE} vs. I_{OUT}



T_{J_RISE} vs. I_{OUT}



Pin Configuration



FC2QFN
3.5mm x 3.75mm

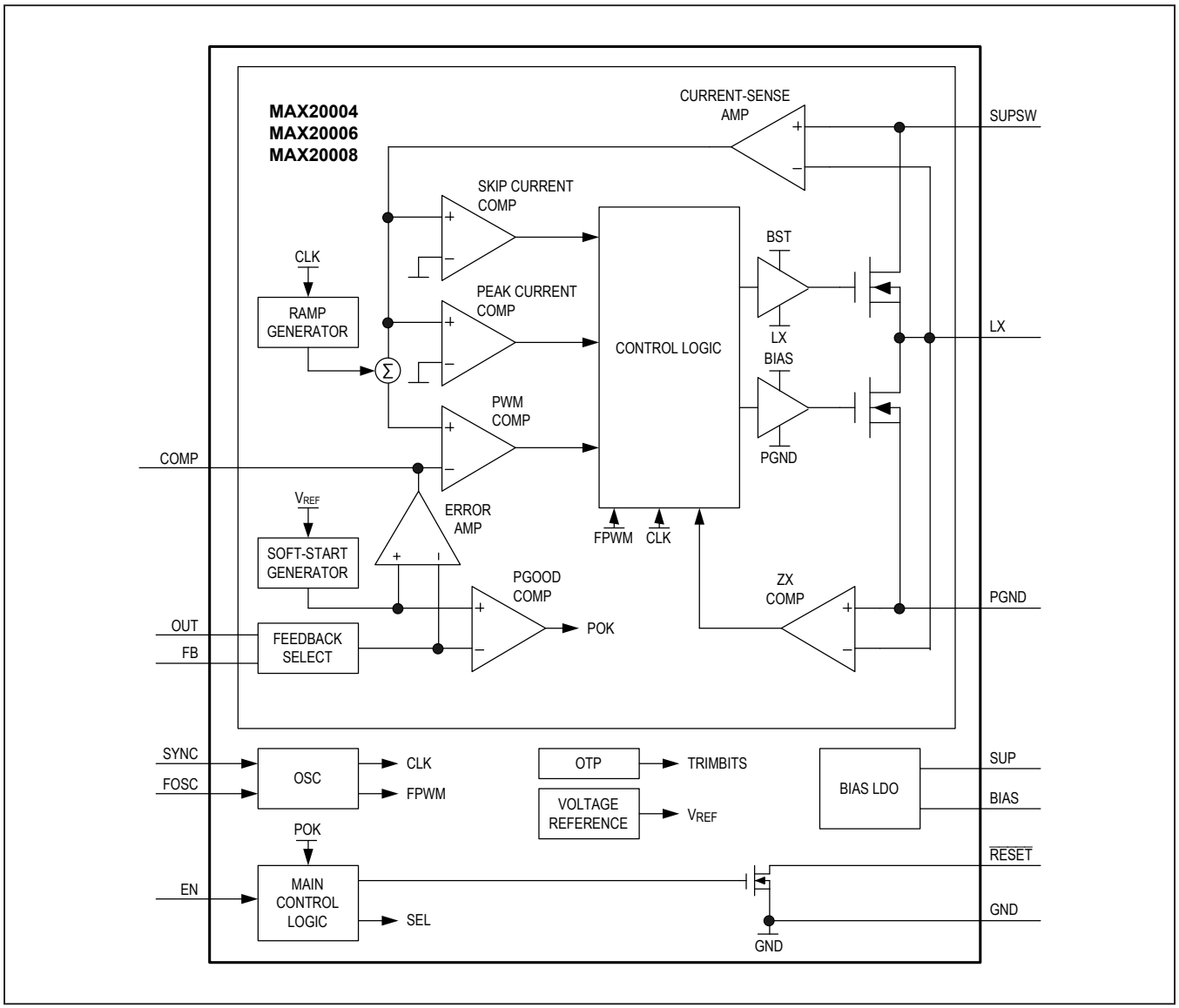
Pin Description

PIN	NAME	FUNCTION
1	OUT	Switching Regulator Output. OUT also provides power to the internal circuitry under certain conditions (see the *Linear Regulator Output (BIAS)* section for details).
2	$\overline{\text{RESET}}$	Open-Drain, Active-Low RESET Output. To obtain a logic signal, pullup $\overline{\text{RESET}}$ with an external resistor.
3	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST for proper operation.
4, 5, 7, 8	PGND	Power Ground. Connect all PGND pins together.
6	LX	Inductor Connection. Connect LX to the switched side of the inductor.
9	SUPSW	Internal High-Side Switch Supply Input. SUPSW provides power to the internal switch. Bypass SUPSW to PGND with 0.1µF and 4.7µF ceramic capacitors. Place the 0.1µF capacitor as close as possible to the SUPSW and PGND pins, followed by the 4.7µF capacitor.
10	SUP	Voltage Supply Input. SUP supplies the internal linear regulator. Connect SUP directly to SUPSW as close as possible to the IC. SUP and SUPSW are connected together internally.
11	EN	SUP Voltage-Compatible Enable Input. Drive EN low to disable the device. Drive EN high to enable the device. For a safe startup, ensure that V_{SUP} > 7.5V when EN is toggled high.
12	SYNC	Connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to BIAS or to an external clock to enable fixed-frequency forced-PWM-mode operation. When driving SYNC externally, do not exceed the BIAS or OUT voltage.
13	BIAS	Linear Regulator Output. BIAS supplies the internal circuitry. Bypass with a minimum 2.2 µF ceramic capacitor to ground. The BIAS pin can transition from 5V to V_{OUT} after startup.
14	GND	Analog Ground

Pin Description (continued)

PIN	NAME	FUNCTION
15	COMP	Error-Amplifier Output. Connect an RC network from COMP to GND for stable operation. See the *Compensation Network* section for more details.
16	FB	Feedback Input. Connect an external resistive divider from OUT to FB and GND to set the output voltage. Connect FB to BIAS to set the output voltage to 5V or 3.3V.
17	FOSC	Resistor-Programmable Switching Frequency Setting Control Input. Connect a resistor from FOSC to GND to set the switching frequency.

Internal Block Diagram



Detailed Description

The MAX20004/MAX20006/MAX2008 are 4A, 6A, and 8A current-mode step-down converters, respectively, with integrated high-side and low-side MOSFETs. The low-side MOSFET enables fixed-frequency FPWM operation in light-load applications. The devices operate with 3.5V to 36V input voltages, while using only 25µA (typ) quiescent current at no load. The switching frequency is resistor programmable from 220kHz to 2.2MHz and can be synchronized to an external clock. The devices' output voltage is available as fixed 5V or 3.3V, or adjustable between 1V and 10V. The wide input voltage range, along with the ability to operate at 99% duty cycle during undervoltage transients, make these devices ideal for automotive applications.

In light-load applications, a logic input (SYNC) allows the devices to operate either in skip mode for reduced current consumption, or fixed-frequency FPWM mode to eliminate frequency variation and help minimize EMI. Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery.

Thermal Considerations

The devices are available in 4A, 6A, or 8A versions; however, the average output-current capability is dependent on several factors. Some of the key factors include the maximum ambient temperature ($T_{A(MAX)}$), switching frequency (f_{SW}), and the number of layers and the size of the PCB. See the *Typical Operating Characteristics* for a guideline.

Wide Input Voltage Range

The devices include two separate supply inputs (SUP and SUPSW) specified for a wide 3.5V to 36V input voltage range. V_{SUP} provides power to the device and V_{SUPSW} provides power to the internal switch. When the device is operating with a 3.5V input supply, conditions such as cold crank can cause the voltage at the SUP and SUPSW pins to drop below the programmed output voltage. Under such conditions, the devices operate in a high duty-cycle mode to facilitate minimum dropout from input to output.

Maximum Duty-Cycle Operation

The devices have an effective maximum duty cycle of 98% (typ). The IC continuously monitors the time between low-side FET switching cycles in both PWM and skip modes. Whenever the low-side FET has not switched for more than 13.5µs (typ), the low-side FET is forced on for 150ns (typ) to refresh the BST capacitor. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

The input voltage at which the device enters dropout can be approximated as:

$$V_{SUP} = \frac{V_{OUT}}{0.98} + I_{OUT} \times R_{HS}$$

where R_{HS} is the high-side switch on-resistance, which should also include the inductor DC resistance for better accuracy.

Linear Regulator Output (BIAS)

The devices include a 5V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. Connect a 2.2µF ceramic capacitor from BIAS to GND. Under certain conditions, the BIAS regulator turns off and the BIAS pin switches to OUT (i.e., switches over) after startup to increase efficiency. For IC versions that are factory trimmed for 3.3V fixed output, BIAS switches to OUT under light load conditions in skip mode only. For IC versions that are factory trimmed for 5V fixed output, the BIAS pin switches to OUT after startup regardless of load or skip/PWM mode. In any case, BIAS only switches over if OUT is between 2.8V and 5.6V. In summary, BIAS can transition from 5V to VOUT after startup depending on load, mode and IC version.

Soft-Start

The devices include a fixed, internal soft-start. Soft-start limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Reset Output ($\overline{RESET}$)

The devices feature an open-drain reset output ($\overline{RESET}$). $\overline{RESET}$ asserts when V_{OUT} drops below the specified falling threshold. $\overline{RESET}$ deasserts when V_{OUT} rises above the specified rising threshold after the specified hold time. Connect $\overline{RESET}$ to the output or I/O voltage of choice (within pin voltage limits) with a pullup resistor.

Synchronization Input (SYNC)

SYNC is a logic-level input used for operating-mode selection and frequency control. Connecting SYNC to BIAS or to an external clock enables forced fixed-frequency (FPWM) operation. Connecting SYNC to GND enables automatic skip-mode operation for light load efficiency. The external clock frequency at SYNC can be higher or lower than the internal clock by 20%. If the external clock frequency is greater than 120% of the internal clock, contact the factory to verify the design. The devices synchronize to the external clock in two cycles. When the external clock signal at SYNC is absent for more than two clock cycles, the devices use the internal clock. There is a diode

between SYNC and BIAS, so it is important when driving SYNC with an external source that the voltage be less than or equal to BIAS (or OUT in the case of switchover). If this cannot be guaranteed, place a series resistor in-line with SYNC ≥ 20kΩ to limit the input current. If EN is low, BIAS is turned off so a voltage should not be present on SYNC without the series resistor.

System Enable (EN)

An enable control input (EN) activates the devices from their low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3.5V.

EN turns on the internal linear (BIAS) regulator. Once V_{BIAS} is above the internal lockout threshold (V_{UVBIAS} = 3V (typ)), the converter activates and the output voltage ramps up with the programmed soft-start time.

A logic-low at EN shuts down the device. During shutdown, the BIAS regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 5µA (typ). Drive EN high to bring the device out of shutdown.

For safe startup, ensure that V_{SUP} > 7.5V when EN is toggled high. In all applications, BIAS capacitance guidelines must be followed to ensure safe operation of the IC.

Note: In all applications, BIAS must start from < 0.3V or > 1.6V during startup.

Spread-Spectrum Option

The devices can be ordered with spread spectrum enabled. See the *Ordering Information/Selector Guide* section. When the spread spectrum is factory enabled, the operating frequency is varied ±3% centered on FOSC. The modulation signal is a triangular wave with a frequency of 4.5kHz at 2.2MHz.

For operations at FOSC values other than 2.2MHz, the modulation signal scales proportionally (e.g., at 400kHz, the modulation frequency reduces by 0.4MHz/2.2MHz).

The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on the SYNC pin and pass any modulation (including spread spectrum) present driving the external clock.

Internal Oscillator (FOSC)

The switching frequency (f_{SW}) is set by a resistor (R_{FOSC}) connected from FOSC to GND. To determine the approximate value of RFOSC for a given fSW, use the graph in the *Typical Operating Characteristics* section or the following equation:

$$R_{FOSC} = \frac{29{,}600}{f_{SW}} - 1.48$$

where f_{SW} is in kHz and RFOSC is in kΩ. For example, a 400kHz switching frequency is set with R_{FOSC} = 72.5kΩ.

Higher frequencies allow designs with lower inductor values and less output capacitance at the expense of reduced efficiency and higher EMI.

Thermal-Shutdown Protection

Thermal shutdown protects the device from excessive operating temperature. When the junction temperature exceeds the specified threshold, an internal sensor shuts down the internal bias regulator and the step-down converter, allowing the IC to cool. The sensor turns the IC on again after the junction temperature cools by the specified hysteresis.

Current Limit/Short-Circuit Protection

The devices feature a current limit that protects them against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the specified LX current-limit threshold. The converter then turns the high-side MOSFET off and the low-side MOSFET on to allow the inductor current to ramp down. Once the inductor current crosses below the current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

A hard short is detected when the output voltage falls below 50% of the target while in current limit. If this occurs, hiccup mode activates, and the output turns off for four times the soft-start time. The output then enters soft-start and powers back up. This repeats indefinitely while the short circuit is present. Hiccup mode is disabled during soft-start.

Overvoltage Protection

If the output voltage exceeds the OV protection rising threshold, the high-side MOSFET turns off and the low-side MOSFET turns on. Normal operation resumes when the output voltage goes below the falling OV threshold.

Applications Information

Maximum Output Current

While there are device versions that supply up to 8A, there are many factors that may limit the average output current to less than the maximum. The devices can be thermally limited based on the selected f_{SW}, number of PCB layers, PCB size, and the maximum ambient temperature. See the *Typical Operating Characteristics* section for guidance on the maximum average current. For a more precise value, the θ_{JA} needs to be measured in the application environment.

Setting the Output Voltage

Connect FB to BIAS for a fixed 5V or 3.3V output voltage. To set the output to other voltages between 1V and 10V, connect a resistive divider from output (OUT) to FB (Figure 1). Select R_{FB2} (FB to GND resistor) less than or equal to 100kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} is the feedback regulation voltage. See the *Electrical Characteristics* table.

Add a capacitor, C_{FB1}, as shown to compensate the pole formed by the divider resistance and FB pin capacitance as follows:

$$C_{FB1} = 10pf \times \left(\frac{R_{FB2}}{R_{FB1}}\right)$$

Note: Applications that use a resistor divider to set output voltages below 4.5V should use IC versions that are factory trimmed for 3.3V fixed output voltage to ensure full output current capability.

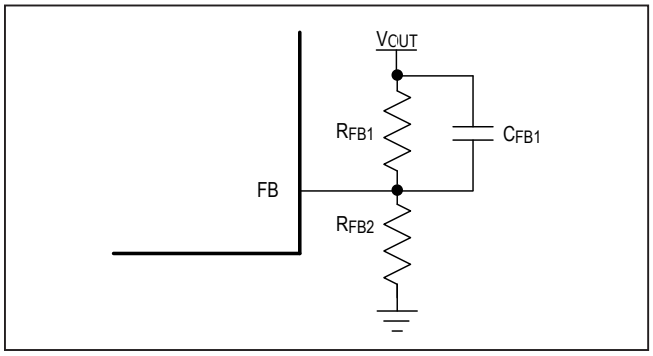


Figure 1. Adjustable Output-Voltage Setting

Forced-PWM and Skip Modes

In forced-PWM (FPWM) mode, the devices switch at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent. At higher load current, the switching frequency becomes fixed and operation is similar to PWM mode. Skip mode helps improve efficiency in light-load applications by allowing switching only when the output voltage falls below a set threshold. Since the effective switching frequency is lower in skip mode at light load, gate charge and switching losses are lower and efficiency is increased.

Inductor Selection

Three key parameters must be considered when selecting an inductor: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The devises are designed to operate with the ratio of inductor peak-to-peak AC current to DC average current (LIR) between 15% and 30% (typ). The switching frequency, input voltage, and output voltage then determine the inductor value as follows:

$$L_{MIN1} = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times I_{MAX} \times 30\%}$$

where V_{SUP} and V_{OUT} are typical values (so that efficiency is optimum for typical conditions) and IMAX is 4A for MAX20004, 6A for MAX20006, and 8A for MAX20008, and f_{SW} is the switching frequency set by R_{FOSC}. Note that IMAX is the maximum rated output current for the device, not the maximum load current in the application.

The next equation ensures that the internal compensating slope is greater than 50% of the inductor current down slope:

$$m \geq \frac{m2}{2}$$

where m is the internal compensating slope and m2 is the sensed inductor current down-slope as follows:

$$m2 = \frac{V_{OUT}}{L} \times R_{CS}$$

where R_{CS} is 0.38 for MAX20004, 0.28 for MAX20006, and 0.21 for MAX20008.

$$m = 1.35\frac{V}{\mu s} \times \frac{f_{SW}}{2.2MHz}$$

Solving for L and using a 1.3 multiplier to account for tolerances in the system:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times m} \times 1.3$$

To satisfy both L_{MIN1} and L_{MIN2}, L_{MIN} must be set to the larger of the two as follows:

$$L_{MIN} = \max(L_{MIN1}, L_{MIN2})$$

The maximum nominal inductor value recommended is 2 times the chosen value from the above formula:

$$L_{MAX} = 2 \times L_{MIN}$$

Select a nominal inductor value based on the following formula:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

The best choice of inductor is usually the standard inductor value closest to L_{NOM}.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input due to high speed switching.

Place a 0.1µF capacitor as close as possible to the SUPSW and PGND pins, followed by a 4.7µF (or larger) ceramic capacitor. A bulk capacitor with higher ESR (such as an electrolytic capacitor) is normally required as well to lower the Q of the front-end circuit and provide the remaining capacitance needed to minimize input voltage ripple.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

$$D = \frac{V_{OUT}}{V_{SUPSW}}$$

where:

I_{OUT} is the maximum output current and D is the duty cycle.

Output Capacitor

The output filter capacitor must have enough capacitance and sufficiently low ESR to meet output-ripple requirements. In addition, the output capacitance must be high enough to maintain the output voltage within specification while the control loop responds to load changes.

When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output-voltage ripple, so the size of the output capacitor depends largely on the maximum ESR allowed to meet the output-voltage ripple specifications as follows:

$$V_{RIPPLE(P-P)} = ESR \times \Delta I_L$$

When using low-ESR (e.g. ceramic) output capacitors, size is usually determined by the capacitance required to maintain the output voltage within specification during load transients and can be estimated as follows:

$$C_{OUT} = \frac{\Delta I}{\Delta V \times 2\pi \times f_C}$$

where ΔI is the load change, ΔV is the allowed voltage droop, and f_C is the loop crossover frequency, which can be assumed to be the lesser of $f_{SW}/10$ or 100kHz. Any calculations involving C_{OUT} should consider capacitance tolerance, temperature, and voltage derating.

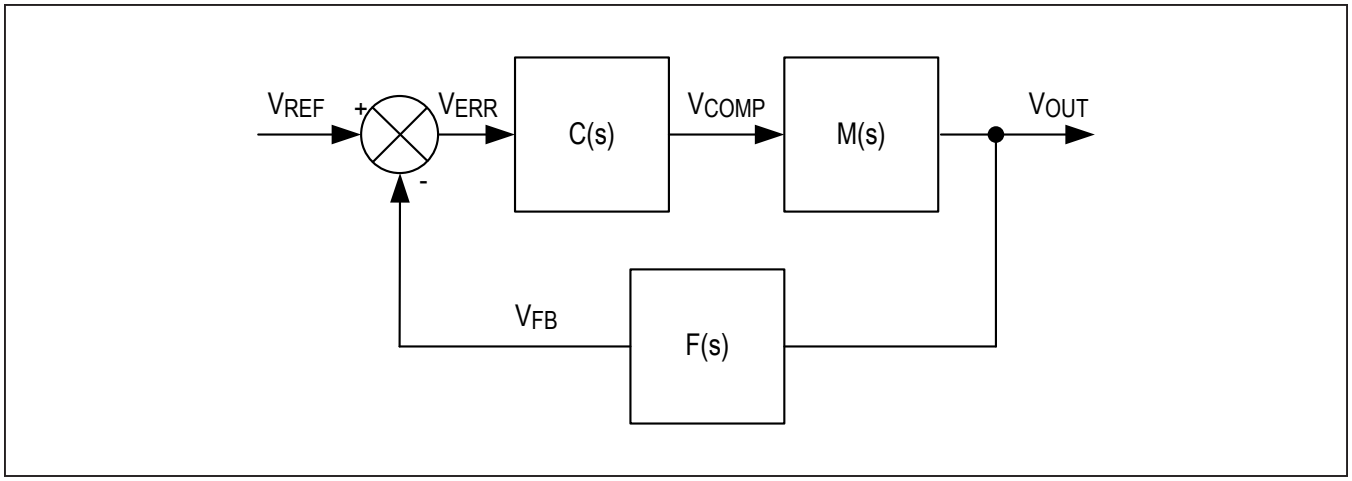


Figure 2. Control System

Compensation Network

The devices use a transconductance amplifier for external frequency compensation. The compensation network in conjunction with the output capacitance primarily determine the loop stability and response. The inductor and the output capacitor are chosen based on performance, size, and cost. The compensation network is used to optimize the loop stability and response.

The converter uses a peak current mode control scheme that regulates the output voltage by forcing the required peak current through the external inductor. The devices use the voltage drop across the high-side MOSFET to sense inductor current. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control.

The final control system can be modeled according to Figure 2 from which the following transfer function is derived:

$$\frac{V_{OUT}(s)}{V_{REF}} = \frac{C(s)M(s)}{1 + F(s)C(s)M(s)}$$

where M(s), C(s) and F(s) are the modulator, compensator and feedback transfer functions, respectively, V_{OUT} is the regulated output voltage and V_{REF} is the internal voltage reference. The product of the modulator, compensator and feedback transfer functions is typically referred to as the loop transfer function.

A simplified condition for stability is that the denominator of the transfer function never equals zero. Accordingly, the loop transfer function should never equal -1, which correspondingly means that the phase must not equal -180 degrees when the magnitude equals 1. In addition, the loop gain should be much less than zero when the phase equals -180 degrees. The frequency at which the magnitude of the loop gain equals 1 (or 0dB) is defined as the crossover frequency (f_C). The difference between the loop phase at the crossover frequency and -180 degrees is defined as the phase margin. The phase margin represents the additional loop phase lag that must occur at the crossover frequency for the system to be unstable. In addition to stability, phase margin is also related to the transient response of the system. Insufficient phase margin causes overshoot and ringing, whereas excessive phase margin causes slow response.

The goal of the system is to have a high crossover frequency, so there is adequate gain to regulate against load transients and other variations in the relevant frequency range, while maintaining adequate phase margin to guard against instability, overshoot, and ringing. In practice, these are fundamentally conflicting criteria that must be managed along with other design goals. According to sampling theory, the crossover frequency cannot exceed one half the switching frequency. In practice, noise and phase margin considerations limit crossover frequency to below one tenth the switching frequency with a practical limit of approximately 100kHz.

The modulator control (COMP) to output transfer function of a current-mode buck regulator can be approximated as follows:

$$\frac{V_{OUT}(s)}{V_{COMP}(s)} = \frac{R_{OUT}}{R_{CS}} \times \frac{\left(1+\frac{s}{\omega z\_esr}\right)}{\left(1+\frac{s}{\omega p\_load}\right)\left(1+\frac{s}{\omega nQ}+\frac{s^2}{\omega n^2}\right)}$$

The first term is the DC gain, which is the quotient of the equivalent load resistance (R_{OUT}) and the current-sense gain (R_{CS}). The numerator is the zero due to the output capacitance (C_{OUT}) and its equivalent series resistance (R_{ESR}), which occurs at the following frequency:

$$fz\_esr = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

The first term in the denominator is the pole due to the load resistance and output capacitance, and occurs at the following frequency:

$$fpload = \frac{1}{2\pi \times R_{OUT} \times C_{OUT}}$$

The last term in the denominator is the sampling double pole, which occurs at 1/2 of the switching frequency ($f_{SW}/2$). The sampling double pole typically occurs at high frequency relative to the crossover frequency and can generally be ignored if there is adequate slope compensation (i.e., low Q). In the typical application, where the ESR is very low due to ceramic output capacitors, the ESR zero also occurs at high frequency and can be ignored as well. In these cases, the transfer function simplifies to the low-frequency dominate pole model as follows:

$$\frac{V_{OUT}(s)}{V_{COMP}(s)} = \frac{R_{OUT}}{R_{CS}} \times \frac{1}{\left(1+\frac{s}{\omega p\_load}\right)}$$

The type 2 compensation network (Figure 3) introduces a zero, a low-frequency pole, and a high frequency pole according to the simplified transfer function below:

$$\frac{V_{COMP}(s)}{V_{ERR}(s)} = G_{EA} \times R_{EA} \times \frac{\left(1+\frac{s}{\omega z\_comp}\right)}{\left(1+\frac{s}{\omega p1\_comp}\right)\left(1+\frac{s}{\omega p2\_comp}\right)}$$

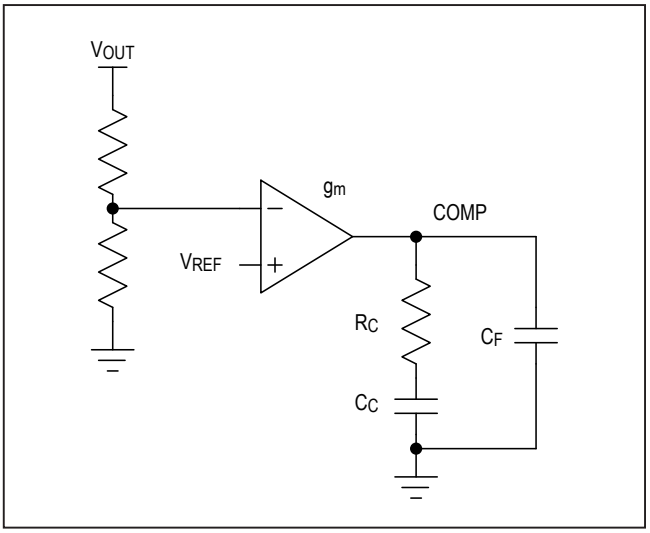


Figure 3. Compensation Network

where G_{EA} and R_{EA} (1.5MΩ typ) are the transconductance and output resistance of the error amplifier, respectively, and the frequency of the poles and zeros are approximately as follows:

$$fz\_comp = \frac{1}{2\pi \times R_C \times C_C}$$

$$fp1\_comp = \frac{1}{2\pi \times R_{EA} \times C_C}$$

$$fp2\_comp = \frac{1}{2\pi \times R_C \times C_F}$$

Compensation resistor, R_C, primarily determines the compensator gain and, thus, crossover frequency, while the separation of the compensator zero and high-frequency pole determine the phase margin. The high-frequency compensator pole is used to cancel the ESR zero or, in the case of very high ESR zero frequency, limit the bandwidth for noise immunity. The low frequency compensator pole is then placed to achieve adequate phase margin and response, typically at the load pole frequency. The selection of C_C, therefore, becomes a tradeoff between phase margin and response.The complete loop transfer

function is the product of the product of the modulator, compensator, and feedback transfer functions as follows:

$$F(s)C(s)M(s) = \frac{V_{REF}}{V_{OUT}} \times \frac{R_{OUT}}{R_{CS}} \times G_{EA} \times R_{EA} \times \frac{\left(1+\frac{s}{\omega z\_esr}\right)\left(1+\frac{s}{\omega z\_comp}\right)}{\left(1+\frac{s}{\omega p\_load}\right)\left(1+\frac{s}{\omega p1\_comp}\right)\left(1+\frac{s}{\omega p2\_comp}\right)}$$

The goal of compensation design is to reduce the loop transfer function to an approximate single-pole system with -20dB/decade gain slope and 90 degrees phase margin at the crossover frequency. To achieve this, the compensator zero is used to cancel the load pole, and the compensator high frequency pole is used to cancel the ESR zero. Assuming these cancellations, the loop transfer function reduces to the following:

$$F(s)C(s)M(s) = \frac{V_{REF}}{V_{OUT}} \times \frac{R_{OUT}}{R_{CS}} \times G_{EA} \times R_{EA} \times \frac{1}{\left(1+\frac{s}{\omega p1\_comp}\right)}$$

To derive the compensation components, the magnitude of the loop gain at the crossover frequency is set equal to 1 and solved for C_C as follows (assuming the magnitude of the compensator pole at the crossover frequency is >>1):

$$\frac{V_{REF}}{V_{OUT}} \times \frac{R_{OUT}}{R_{CS}} \times G_{EA} \times R_{EA} \times \frac{1}{(2\pi \times f_C \times R_{EA} \times C_C)} = 1$$

$$C_C = \frac{V_{REF} \times R_{OUT} \times G_{EA}}{2\pi \times f_C \times V_{OUT} \times R_{CS}}$$

Setting the compensator zero frequency equal to the load pole frequency and solving for R_C yields:

$$\frac{1}{2\pi \times R_C \times C_C} = \frac{1}{2\pi \times R_{OUT} \times C_{OUT}}$$

$$R_C = \frac{2\pi \times C_{OUT} \times R_{CS} \times V_{OUT} \times f_C}{V_{REF} \times G_{EA}}$$

The above leads to an alternative equation for C_C as follows:

$$C_C = \frac{R_{OUT} \times C_{OUT}}{R_C}$$

Finally, setting the high-frequency compensator pole equal to the minimum of the ESR zero frequency or 1/2 the switching frequency and solving for C_F yields:

$$\frac{1}{2\pi \times R_C \times C_F} = \text{Min}\left(\frac{f_{SW}}{2}, \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}\right)$$

$$C_F = \frac{1}{2\pi \times R_C \times \text{Min}\left(\frac{f_{SW}}{2}, \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}\right)}$$

The above equation leads to the following compensation design procedure:

1) Select a crossover frequency equal to one tenth of the switching frequency (f_{SW}/10) or 100kHz, whichever is lower.
2) Calculate and select the compensation resistor, R_C.
3) Calculate and select the compensation capacitor, C_C.
4) Calculate and select compensation capacitor C_F.
5) Evaluate the gain and phase of the final loop transfer function at the crossover frequency and adjust crossover frequency and/or compensation as required.
6) Verify the final design with transient line/load response testing and gain-phase measurements and adjust as required.

PCB Layout Guidelines

Careful PCB layout is critical for stability, low-noise/EMI and overall performance. Use a multilayer board whenever possible for better noise immunity and power dissipation. See Figure 4 for the following guidelines for good PCB layout:

1) Use the correct footprint for the IC and place as many copper planes as possible under the IC footprint to ensure efficient heat transfer.
2) Place the ceramic input bypass capacitors (C_{BP} and C_{IN}) as close as possible to the SUPSW and PGND pins on the same side as the IC. Use low-impedance connections (no vias or other discontinuities) between the capacitors and IC pins. C_{BP} should be located closest to the IC and should have very good high-frequency performance (small package size, low inductance, and high. Use flexible terminations or other technologies instead of series capacitors for these functions if failure modes are a concern. This approach provides the best EMI rejection and minimizes internal noise on the device, which can degrade performance.
3) Place the inductor (L), output capacitors (C_{OUT}), boost capacitor (C_{BST}) and BIAS capacitor (C_B) on the same side as the IC in such a way as to minimize the area enclosed by the current loops. Place the inductor (L) as close as possible to the IC LX pin and minimize the area of the LX node. Place the output capacitors (COUT) near the inductor and the ground side of COUT near the CIN ground connection so as to minimize the current the loop area. Place the BIAS capacitor (CB) next to the BIAS pin.
4) Use a contiguous copper GND plane on the layer next to the IC to provide an image plane and shield the entire circuit. GND should also be poured around the entire circuit on the top side. Use a single GND: do not separate or isolate PGND and GND connections with separate planes or copper areas. Ensure that all heat-dissipating components have adequate connections to copper for cooling. Use multiple vias to interconnect GND planes/areas for low impedance and maximum heat dissipation. Place vias at the GND terminals of the IC, input/output/bypass capacitors, and other components.
5) Place the compensation network (CF, CC, RC) near the COMP pin so that the ground connections are as short as possible to the GND pin. Keep high frequency signals away from these components.
6) Place the oscillator set resistor (RF) near the FSET pin so that the ground connection is as short as possible to the GND pin. Keep high-frequency signals away from this component.
7) Place the feedback resistor-divider (if used) near the IC and route the feedback and OUT connections away from the inductor and LX node and other noisy signals.

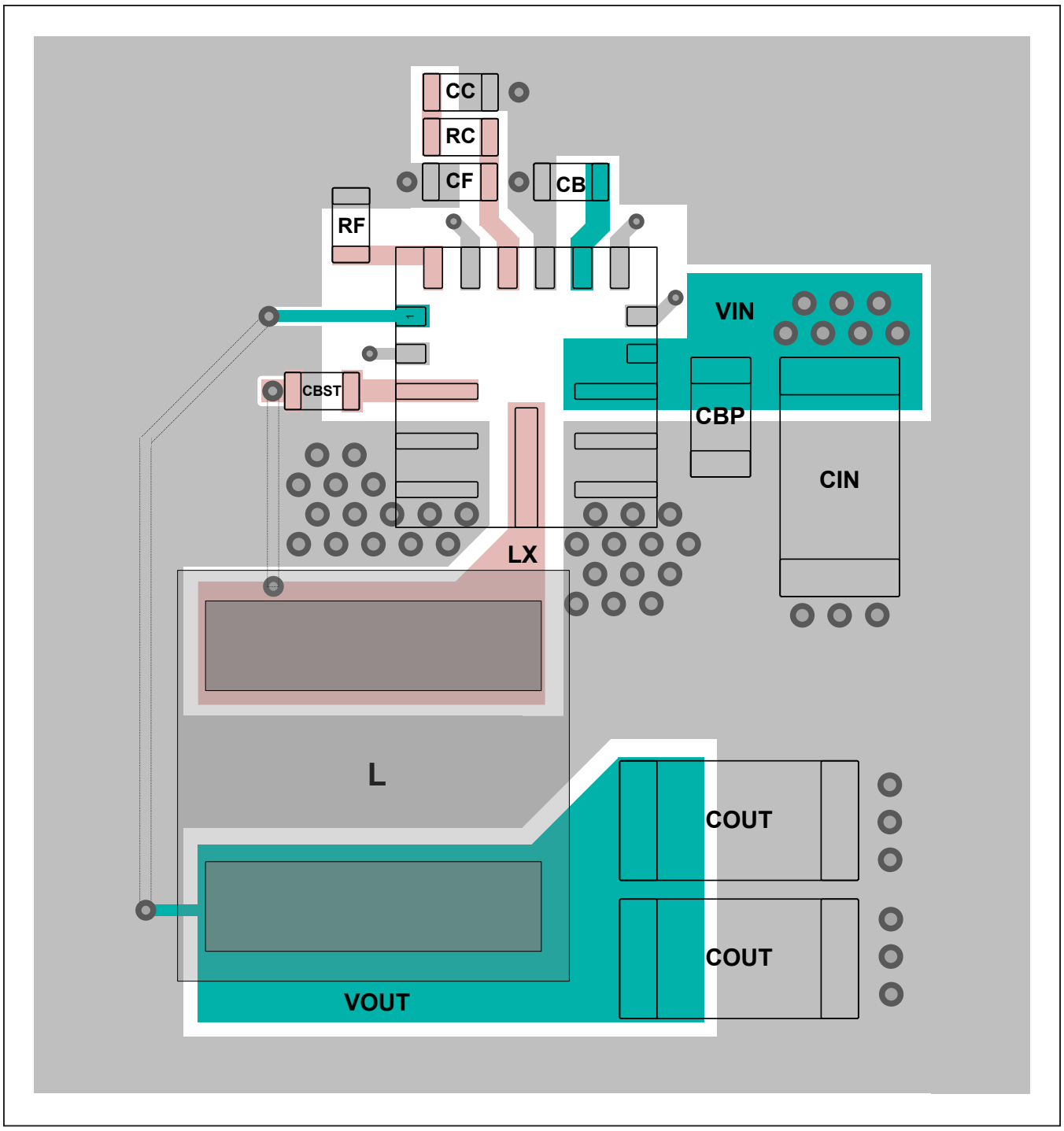


Figure 4. Simplified Layout Example

Ordering Information/Selector Guide

PART	V_{OUT} (FB TIED TO BIAS)	V_{OUT} (EXTERNAL RESISTOR-DIVIDER) (V)	MAXIMUM OPERATING CURRENT (A)	T_{HOLD} (ms)	SPREAD SPECTRUM
MAX20004AFOA/VY+	5.0	4.5–10	4	0.2	Off
MAX20004AFOB/VY+	3.3	1–10	4	0.2	Off
MAX20004AFOC/VY+	5.0	4.5–10	4	0.2	On
MAX20004AFOD/VY+	3.3	1–10	4	0.2	On
MAX20006AFOA/VY+	5.0	4.5–10	6	0.2	Off
MAX20006AFOB/VY+	3.3	1–10	6	0.2	Off
MAX20006AFOC/VY+	5.0	4.5–10	6	0.2	On
MAX20006AFOD/VY+	3.3	1–10	6	0.2	On
MAX20008AFOA/VY+	5.0	4.5–10	8	0.2	Off
MAX20008AFOB/VY+	3.3	1–10	8	0.2	Off
MAX20008AFOC/VY+	5.0	4.5–10	8	0.2	On
MAX20008AFOD/VY+	3.3	1–10	8	0.2	On

For variants with different options, contact factory.
/V Denotes an automotive-qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—
1	5/18	Removed future product status from MAX20006AFOA/VY+ and MAX20008AFOC/VY+ variants in the *Ordering Information/Selector Guide* table	19
2	8/18	Updated the *Package Information* table, and *Reset Output ($\overline{RESET}$), Setting the Output Voltage, Output Capacitor,* and *Compensation Network* sections ; reformatted the *Typical Operating Characteristics* charts; replaced TOC17 and TOC18; and removed future product designation from MAX2006AFOB/VY+, MAX2006AFOB/VY+, MAX2006AFOB/VY+, MAX2006AFOB/VY+, MAX2006AFOB/VY+, and MAX2006AFOB/VY+	2, 5–7, 10 12–16, 19
3	11/18	Removed future product status from MAX20004AFOA/VY+, MAX20004AFOB/VY+, MAX20004AFOC/VY+, and MAX20004AFOD/VY+ variants in the *Ordering Information/Selector Guide* table	19
4	1/19	Updated land pattern number in *Package Information* table	2
5	1/19	Updated thermal resistance values in *Package Information* table and added V_{OUT} (external resistor-divider) column to *Ordering Information/Selector Guide* table	2, 19
6	2/19	Added “automotive” to product description	1–19
7	9/19	Updated *Typical Application Circuit*, *Pin Description*, and *Detailed Description*	1, 8, 11
8	11/19	Updated *Pin Description*, and *Detailed Description*	8, 11

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