



FEATURES

Isolated, RS-485/RS-422 transceiver, configurable as half- or full-duplex

±15 kV ESD protection on RS-485 input/output pins

500 kbps data rate

Complies with ANSI TIA/EIA RS-485-A-1998 and

ISO 8482: 1987(E)

Suitable for 5 V or 3.3 V operation (V_{DD1})

High common-mode transient immunity: >25 kV/ μ s

True fail-safe receiver inputs

256 nodes on the bus

Thermal shutdown protection

[Safety and regulatory approvals](#)

UL recognition

5000 V rms isolation voltage for 1 minute per UL1577

VDE certificate of conformity

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12

Reinforced insulation, $V_{IORM} = 849 V_{PEAK}$

CSA Component Acceptance Notice 5A

IEC 60950-1: 390 V rms (reinforced)

Operating temperature range: -40°C to +85°C

Wide body, 16-lead SOIC package

APPLICATIONS

Isolated RS-485/RS-422 interfaces

Industrial field networks

INTERBUS

Multipoint data transmission systems

GENERAL DESCRIPTION

The [ADM2484E](#) is an isolated data transceiver with ±15 kV ESD protection suitable for high speed, half- or full-duplex communication on multipoint transmission lines. For half-duplex operation, the transmitter outputs and receiver inputs share the same transmission line. Transmitter Output Pin Y links externally to Receiver Input Pin A, and Transmitter Output Pin Z links externally to Receiver Input Pin B.

Designed for balanced transmission lines, the [ADM2484E](#) complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482: 1987(E). The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a three-state differential line driver, and a differential input receiver into a single package.

FUNCTIONAL BLOCK DIAGRAM

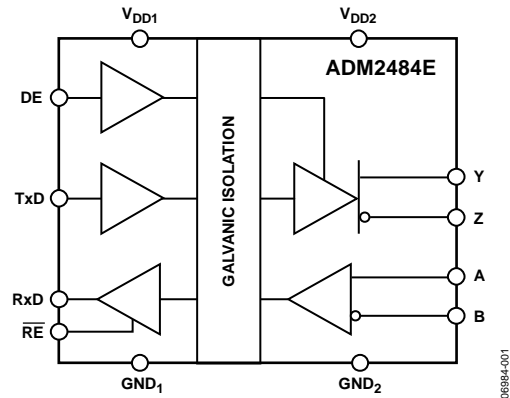


Figure 1.

069884-001

The differential transmitter outputs and receiver inputs feature electrostatic discharge circuitry that provides protection up to ±15 kV using the human body model (HBM). The logic side of the device can be powered with either a 5 V or a 3.3 V supply, whereas the bus side requires an isolated 3.3 V supply.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention causes excessive power dissipation.

Rev. G

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TABLE OF CONTENTS

| | | | |
|---------------------------------------------------|---|-------------------------------------|----|
| Features | 1 | Test Circuits..... | 10 |
| Applications..... | 1 | Switching Characteristics | 11 |
| Functional Block Diagram | 1 | Circuit Description..... | 12 |
| General Description | 1 | Electrical Isolation..... | 12 |
| Revision History | 2 | Truth Tables..... | 12 |
| Specifications..... | 3 | Thermal Shutdown | 13 |
| Timing Specifications | 4 | True Fail-Safe Receiver Inputs..... | 13 |
| Package Characteristics | 4 | Magnetic Field Immunity..... | 13 |
| Regulatory Information..... | 4 | Applications Information | 14 |
| Insulation and Safety-Related Specifications..... | 5 | Isolated Power Supply Circuit | 14 |
| VDE 0884 Insulation Characteristics | 5 | PC Board Layout | 14 |
| Absolute Maximum Ratings..... | 6 | Typical Applications..... | 15 |
| ESD Caution..... | 6 | Outline Dimensions | 16 |
| Pin Configuration and Function Descriptions..... | 7 | Ordering Guide | 16 |
| Typical Performance Characteristics | 8 | | |

REVISION HISTORY

5/2018—Rev. F to Rev. G

| | |
|----------------------------------|---|
| Change to Features Section | 1 |
| Changes to Table 4..... | 4 |

11/2015—Rev. E to Rev. F

| | |
|----------------------------------------------|---|
| Added Table 8; Renumbered Sequentially | 6 |
|----------------------------------------------|---|

3/2015—Rev. D to Rev. E

| | |
|---------------------------------------------------------|---|
| Changes to CTI Value and Isolation Group, Table 5 | 5 |
|---------------------------------------------------------|---|

3/2014—Rev. C to Rev. D

| | |
|--------------------------------------------------------------------------------|---|
| Changes to Features Section..... | 1 |
| Changed V_{IORM} from $846 V_{PEAK}$ to $849 V_{PEAK}$, Table 4 | 4 |
| Changes to VDE 0884 Insulation Characteristics Section..... | 5 |
| Additional T_J Junction Temperature of 110°C , Table 7 | 6 |

11/2010—Rev. B to Rev. C

| | |
|--------------------------------------------------------------------------|----|
| Changes to Features Section | 1 |
| Changes to Table 4..... | 4 |
| Change to Maximum Working Insulation Voltage Parameter, Table 6 | 5 |
| Changes to Figure 30 and Figure 31..... | 15 |
| Updated Outline Dimensions | 16 |
| Changes to Ordering Guide | 16 |

3/2010—Rev. A to Rev. B

| | |
|-----------------------------------------------------------------------------|---|
| Changes to Minimum External Tracking (Creepage) Parameter, Table 5 | 5 |
|-----------------------------------------------------------------------------|---|

3/2009—Rev. 0 to Rev. A

| | |
|---------------------------|----|
| Changes to Figure 28..... | 14 |
|---------------------------|----|

5/2008—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective grounds, $3.0\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ and $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, all minimum/maximum specifications apply over the entire recommended operation range, all typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|------------------------------------------------------------------|------------------|-----------------------|-----------------|----------------------|-------------------|-------------------------------------------------------------------------------------------------------|
| SUPPLY CURRENT | | | | | | |
| Power Supply Current, Logic Side TxD/RxD Data Rate = 500 kbps | I_{DD1} | | | 2.0 | mA | Unloaded |
| | | | | 2.0 | mA | $V_{DD2} = 3.6\text{ V}$, half duplex configuration, $R_{TERMINATION} = 120\ \Omega$, see Figure 20 |
| Power Supply Current, Bus Side TxD/RxD Data Rate = 500 kbps | I_{DD2} | | | 3.0 | mA | Unloaded |
| | | | | 40 | mA | $V_{DD2} = 3.6\text{ V}$, half duplex configuration, $R_{TERMINATION} = 120\ \Omega$, see Figure 20 |
| DRIVER | | | | | | |
| Differential Outputs | | | | | | |
| Differential Output Voltage | $ V_{OD} $ | 2.0 | | 3.6 | V | Loaded, $R_L = 100\ \Omega$ (RS-422), see Figure 14 |
| | | 1.5 | | 3.6 | V | $R_L = 54\ \Omega$ (RS-485), see Figure 14 |
| | | 1.5 | | 3.6 | V | $-7\text{ V} \leq V_{TEST} \leq 12\text{ V}$, see Figure 15 |
| $\Delta V_{OD} $ for Complementary Output States | $\Delta V_{OD} $ | | | 0.2 | V | $R_L = 54\ \Omega$ or $100\ \Omega$, see Figure 14 |
| Common-Mode Output Voltage | V_{OC} | | | 3.0 | V | $R_L = 54\ \Omega$ or $100\ \Omega$, see Figure 14 |
| $\Delta V_{OC} $ for Complementary Output States | $\Delta V_{OC} $ | | | 0.2 | V | $R_L = 54\ \Omega$ or $100\ \Omega$, see Figure 14 |
| Output Leakage Current (Y, Z Pins) | I_o | | | 30 | μA | $DE = 0\text{ V}$, $V_{DD2} = 0\text{ V}$ or 3.3 V , $V_{IN} = 12\text{ V}$ |
| | | -30 | | | μA | $DE = 0\text{ V}$, $V_{DD2} = 0\text{ V}$ or 3.3 V , $V_{IN} = -7\text{ V}$ |
| Short-Circuit Output Current | I_{OS} | | | 250 | mA | |
| Logic Inputs (DE, \overline{RE} , TxD) | | | | | | |
| Input Threshold Low | V_{IL} | $0.25 \times V_{DD1}$ | | | V | |
| Input Threshold High | V_{IH} | | | $0.7 \times V_{DD1}$ | V | |
| Input Current | I_i | -10 | +0.01 | +10 | μA | |
| RECEIVER | | | | | | |
| Differential Inputs | | | | | | |
| Differential Input Threshold Voltage | V_{TH} | -200 | -125 | -30 | mV | $-7\text{ V} < V_{CM} < +12\text{ V}$ |
| Input Voltage Hysteresis | V_{HYS} | | 15 | | mV | $V_{OC} = 0\text{ V}$ |
| Input Current (A, B) | I_i | | | 125 | μA | $DE = 0\text{ V}$, $V_{DD} = 0\text{ V}$ or 3.6 V , $V_{IN} = 12\text{ V}$ |
| | | -100 | | | | μA |
| Line Input Resistance | R_{IN} | 96 | | | k Ω | $-7\text{ V} < V_{CM} < +12\text{ V}$ |
| Tristate Leakage Current | I_{OZR} | | | ± 1 | μA | $V_{DD1} = 5\text{ V}$, $0\text{ V} < V_{OUT} < V_{DD1}$ |
| Logic Outputs | | | | | | |
| Output Voltage Low | V_{OLRXD} | | 0.2 | 0.4 | V | $I_{ORXD} = 1.5\text{ mA}$, $V_A - V_B = -0.2\text{ V}$ |
| Output Voltage High | V_{OHRXD} | $V_{DD1} - 0.3$ | $V_{DD1} - 0.2$ | | V | $I_{ORXD} = -1.5\text{ mA}$, $V_A - V_B = +0.2\text{ V}$ |
| Short-Circuit Current | | | | 100 | mA | |
| COMMON-MODE TRANSIENT IMMUNITY ¹ | | 25 | | | kV/ μs | $V_{CM} = 1\text{ kV}$, transient magnitude = 800 V |

¹ CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONST_A = -40°C to +85°C.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|-----------------------------------------------------------------------------|---------------------------------------|-----|-----|------|------|------------------------------------------------------------------------------------------------|
| DRIVER | | | | | | |
| Propagation Delay | t _{DPLH} , t _{DPHL} | 250 | | 700 | ns | R _L = 54 Ω, C _{L1} = C _{L2} = 100 pF, see Figure 16 and Figure 21 |
| Differential Driver Output Skew (t _{DPLH} - t _{DPHL}) | t _{DSKEW} | | | 100 | ns | R _L = 54 Ω, C _{L1} = C _{L2} = 100 pF, see Figure 16 and Figure 21 |
| Rise Time/Fall Time | t _{DR} , t _{DF} | 200 | 450 | 1100 | ns | R _L = 54 Ω, C _{L1} = C _{L2} = 100 pF, see Figure 16 and Figure 21 |
| Enable Time | t _{ZL} , t _{ZH} | | | 1.5 | μs | R _L = 110 Ω, C _L = 50 pF, see Figure 18 and Figure 22 |
| Disable Time | t _{LZ} , t _{HZ} | | | 200 | ns | R _L = 110 Ω, C _L = 50 pF, see Figure 18 and Figure 22 |
| RECEIVER | | | | | | |
| Propagation Delay | t _{PLH} , t _{PHL} | | | 200 | ns | C _L = 15 pF, see Figure 17 and Figure 23 |
| Pulse Width Distortion, PWD = t _{PLH} - t _{PHL} | t _{PWD} | | | 30 | ns | C _L = 15 pF, see Figure 17 and Figure 23 |
| Enable Time | t _{ZL} , t _{ZH} | | | 13 | ns | R _L = 1 kΩ, C _L = 15 pF, see Figure 19 and Figure 24 |
| Disable Time | t _{LZ} , t _{HZ} | | | 13 | ns | R _L = 1 kΩ, C _L = 15 pF, see Figure 19 and Figure 24 |

PACKAGE CHARACTERISTICS

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--------------------------------------------|------------------|-----|------------------|-----|------|-----------------------------------------------------|
| RESISTANCE | | | | | | |
| Resistance (Input-to-Output) ¹ | R _{I-O} | | 10 ¹² | | Ω | |
| CAPACITANCE | | | | | | |
| Capacitance (Input-to-Output) ¹ | C _{I-O} | | 3 | | pF | f = 1 MHz |
| Input Capacitance ² | C _i | | 4 | | pF | |
| THERMAL RESISTANCE | | | | | | |
| Input IC Junction-to-Case | θ _{JCI} | | 33 | | °C/W | Thermocouple located at center of package underside |
| Output IC Junction-to-Case | θ _{JCO} | | 28 | | °C/W | |

¹ Device considered a 2-terminal device: Pin 1 to Pin 8 are shorted together and Pin 9 to Pin16 are shorted together.² Input capacitance is from any input data pin to ground.**REGULATORY INFORMATION**

Table 4.

| UL ¹ | CSA | VDE ² |
|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A, CSA 60950-1-07+A1+A2 and IEC 60950-1 second edition +A1+A2: Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 390 V rms (552 V peak) CSA 61010-1-12+A1 and IEC 61010-1 third edition: Basic 600 V rms, Overvoltage Category III Reinforced 300 V rms, Overvoltage Category III | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ² |
| 5000 V rms Isolation Voltage | | Reinforced insulation, 849 V _{PEAK} |

¹ In accordance with UL1577, each ADM2484E is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 μA).² In accordance with DIN V VDE V 0884-10, each ADM2484E is proof tested by applying an insulation test voltage ≥ 1590 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

| Parameter | Symbol | Value | Unit | Conditions |
|--------------------------------------------------|--------|-------|--------|----------------------------------------------------------------------------------|
| Rated Dielectric Insulation Voltage | | 5000 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 7.7 | mm min | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 7.6 | mm min | Measured from input terminals to output terminals, shortest distance along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 | mm min | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

VDE 0884 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits. An asterisk (*) on a package denotes VDE 0884 approval for 849 V_{PEAK} working voltage.

Table 6.

| Description | Conditions | Symbol | Characteristic | Unit |
|----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|------------------------|------------------|-------------------|
| CLASSIFICATIONS | | | | |
| Installation Classification per DIN VDE 0110 for Rated Mains Voltage | | | I to IV | |
| ≤300 V rms | | | I to II | |
| ≤450 V rms | | | I to II | |
| ≤600 V rms | | | 40/105/21 | |
| Climatic Classification | | | 2 | |
| Pollution Degree | DIN VDE 0110, see Table 1 | | | |
| VOLTAGE | | | | |
| Maximum Working Insulation Voltage | | V _{IORM} | 849 | V _{PEAK} |
| Input-to-Output Test Voltage | | V _{PR} | | |
| Method b1 | V _{IORM} × 1.875 = V _{PR} , 100% production tested, t _m = 1 sec, partial discharge < 5 pC | | 1590 | V _{PEAK} |
| Method a | | | | |
| After Environmental Tests, Subgroup 1 | V _{IORM} × 1.6 = V _{PR} , t _m = 60 sec, partial discharge < 5 pC | | 1357 | V _{PEAK} |
| After Input and/or Safety Test, Subgroup 2/Subgroup 3 | V _{IORM} × 1.2 = V _{PR} , t _m = 60 sec, partial discharge < 5 pC | | 1018 | V _{PEAK} |
| Highest Allowable Overvoltage | (Transient overvoltage, t _{TR} = 10 sec) | V _{TR} | 6000 | V _{PEAK} |
| SAFETY-LIMITING VALUES | Maximum value allowed in the event of a failure, see Figure 9 | | | |
| Case Temperature | | T _S | 150 | °C |
| Input Current | | I _{S, INPUT} | 265 | mA |
| Output Current | | I _{S, OUTPUT} | 335 | mA |
| Insulation Resistance at T _S | V _{IO} = 500 V | R _S | >10 ⁹ | Ω |

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. Each voltage is relative to its respective ground.

Table 7.

| Parameter | Rating |
|-----------------------------------------------|---------------------------------------------|
| V_{DD1} | -0.5 V to +7 V |
| V_{DD2} | -0.5 V to +6 V |
| Logic Input Voltages | -0.5 V to $V_{DD1} + 0.5$ V |
| Bus Terminal Voltages | -9 V to +14 V |
| Logic Output Voltages | -0.5 V to $V_{DD1} + 0.5$ V |
| Average Output Current per Pin | ± 35 mA |
| ESD (Human Body Model) on A, B, Y, and Z Pins | ± 15 kV |
| Storage Temperature Range | -55°C to $+150^\circ\text{C}$ |
| Ambient Operating Temperature Range | -40°C to $+85^\circ\text{C}$ |
| θ_{JA} Thermal Impedance | 73°C/W |
| T_J Junction Temperature | 110°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination.

Table 8. Maximum Continuous Working Voltage¹

| Parameter | Max | Unit | Reference Standard |
|-----------------------|------|------------|---------------------------------------------------------------------------------------|
| AC Voltage | | | |
| Bipolar Waveform | | | |
| Basic Insulation | 565 | V_{PEAK} | 50-year minimum lifetime |
| Reinforced Insulation | 565 | V_{PEAK} | 50-year minimum lifetime |
| Unipolar Waveform | | | |
| Basic Insulation | 1131 | V_{PEAK} | 50-year minimum lifetime |
| Reinforced Insulation | 864 | V_{PEAK} | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| DC Voltage | | | |
| Basic Insulation | 1066 | V_{PEAK} | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 529 | V_{PEAK} | Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1 |

¹ Refers to continuous voltage magnitude imposed across the isolation barrier.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

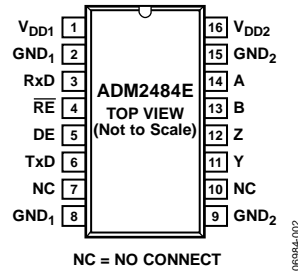


Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | V _{DD1} | Power Supply (Logic Side). Decoupling capacitor to GND ₁ required; capacitor value should be between 0.01 μ F and 0.1 μ F. |
| 2 | GND ₁ | Ground (Logic Side). |
| 3 | RxD | Receiver Output. |
| 4 | $\overline{\text{RE}}$ | Receiver Enable Input. Active low logic input. When this pin is low, the receiver is enabled; when this pin is high, the receiver is disabled. |
| 5 | DE | Driver Enable Input. Active high logic input. When this pin is high, the driver (transmitter) is enabled; when this pin is low, the driver is disabled. |
| 6 | TxD | Transmit Data. |
| 7 | NC | No Connect. This pin must be left floating. |
| 8 | GND ₁ | Ground (Logic Side). |
| 9 | GND ₂ | Ground (Bus Side). |
| 10 | NC | No Connect. This pin must be left floating. |
| 11 | Y | Driver Noninverting Output. |
| 12 | Z | Driver Inverting Output. |
| 13 | B | Receiver Inverting Input. |
| 14 | A | Receiver Noninverting Input. |
| 15 | GND ₂ | Ground (Bus Side). |
| 16 | V _{DD2} | Power Supply (Bus Side). Decoupling capacitor to GND ₂ required; capacitor value should be between 0.01 μ F and 0.1 μ F. |

TYPICAL PERFORMANCE CHARACTERISTICS

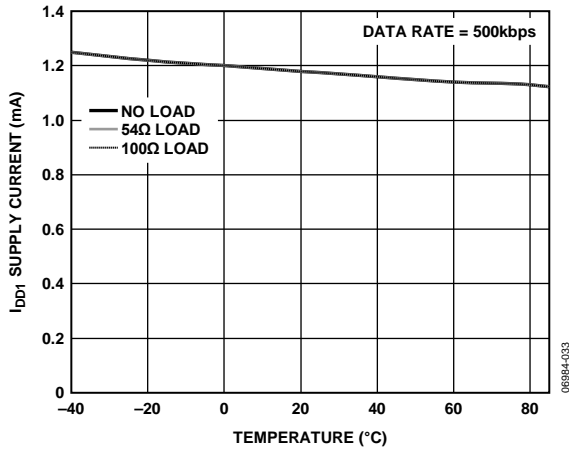


Figure 3. I_{DD1} Supply Current vs. Temperature (See Figure 20)

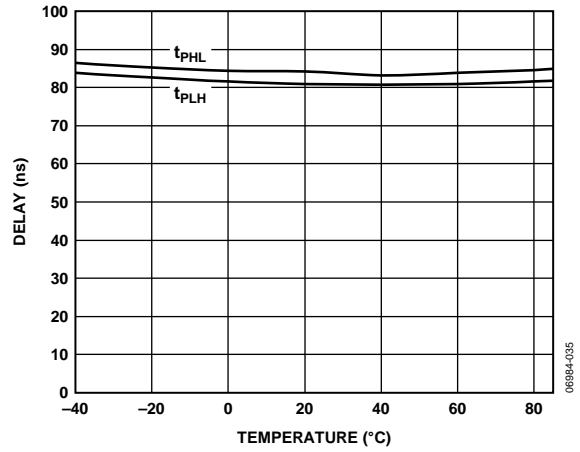


Figure 6. Receiver Propagation Delay vs. Temperature

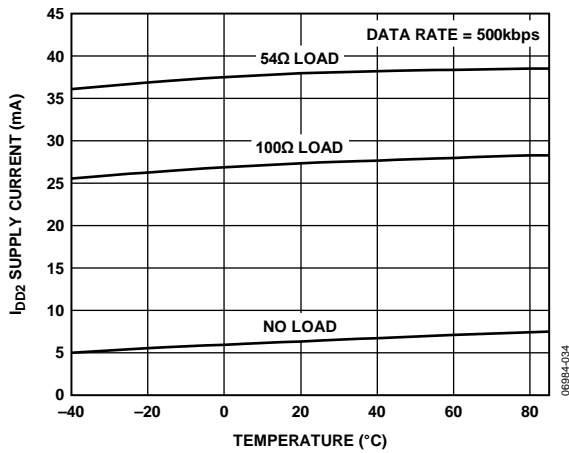


Figure 4. I_{DD2} Supply Current vs. Temperature (See Figure 20)

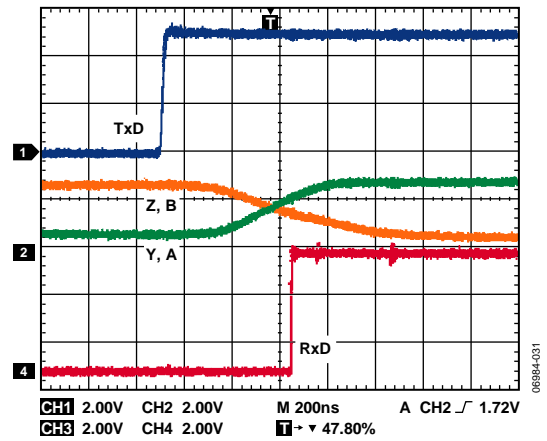


Figure 7. Driver/Receiver Propagation Delay, Low to High ($R_L = 54 \Omega, C_{L1} = C_{L2} = 100 \text{ pF}$)

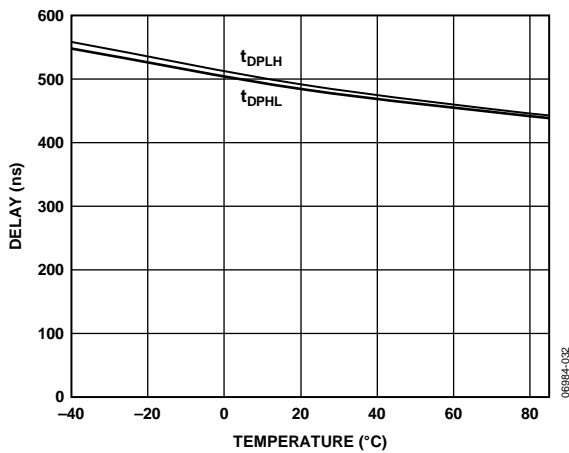


Figure 5. Driver Propagation Delay vs. Temperature

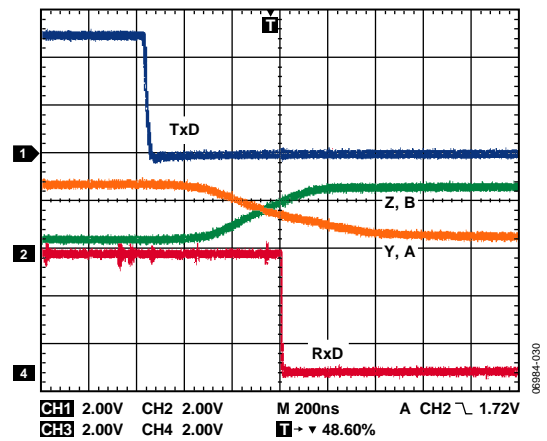


Figure 8. Driver/Receiver Propagation Delay, High to Low ($R_L = 54 \Omega, C_{L1} = C_{L2} = 100 \text{ pF}$)

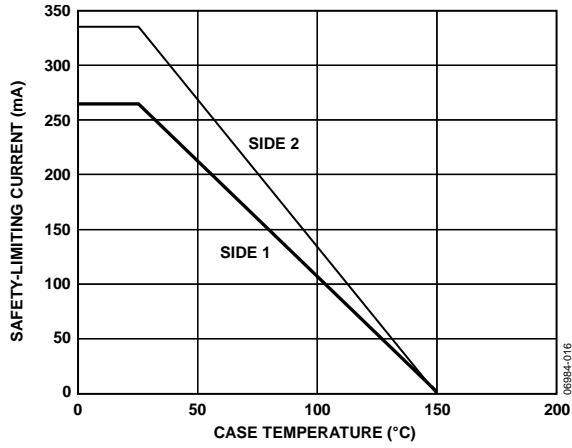


Figure 9. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

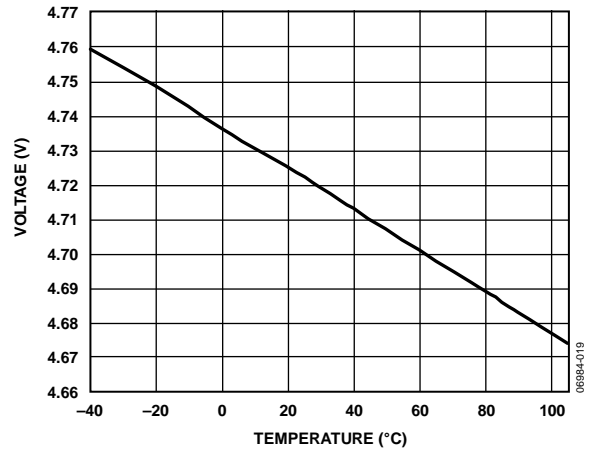


Figure 12. Receiver Output High Voltage vs. Temperature, $I_{RxD} = -4$ mA

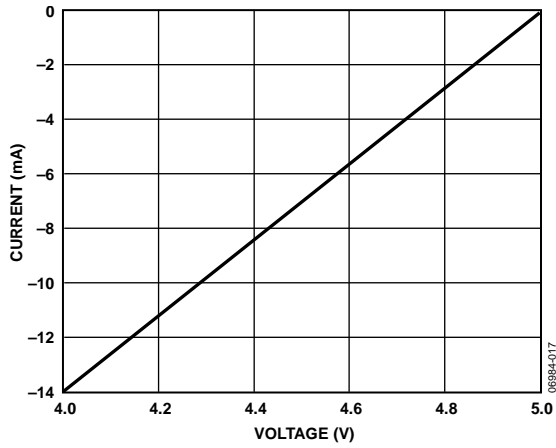


Figure 10. Output Current vs. Receiver Output High Voltage

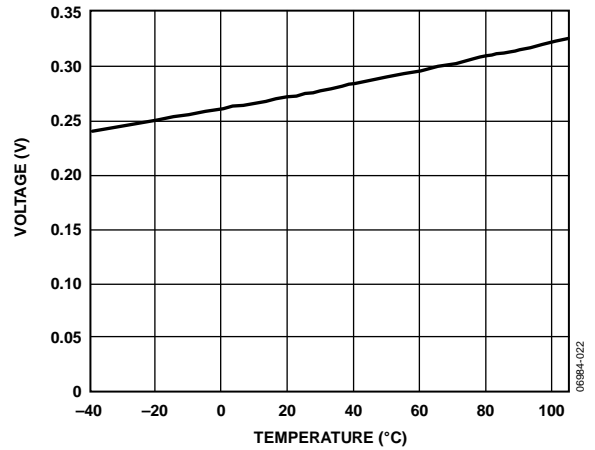


Figure 13. Receiver Output Low Voltage vs. Temperature, $I_{RxD} = +4$ mA

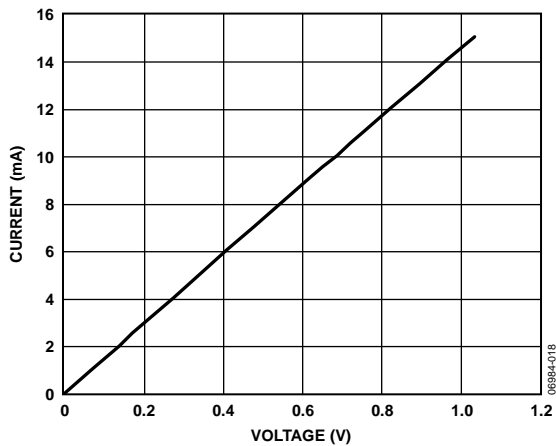


Figure 11. Output Current vs. Receiver Output Low Voltage

TEST CIRCUITS

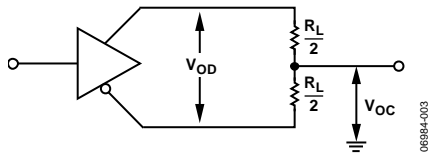


Figure 14. Driver Voltage Measurement

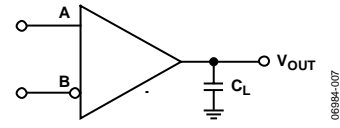


Figure 17. Receiver Propagation Delay

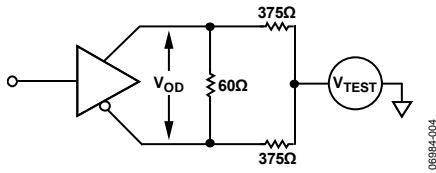


Figure 15. Driver Voltage Measurement

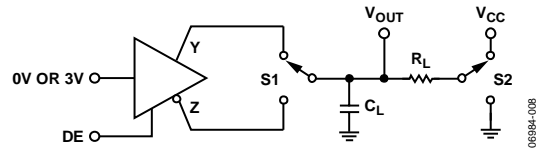


Figure 18. Driver Enable/Disable

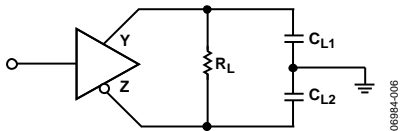


Figure 16. Driver Propagation Delay

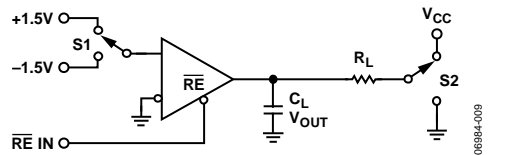


Figure 19. Receiver Enable/Disable

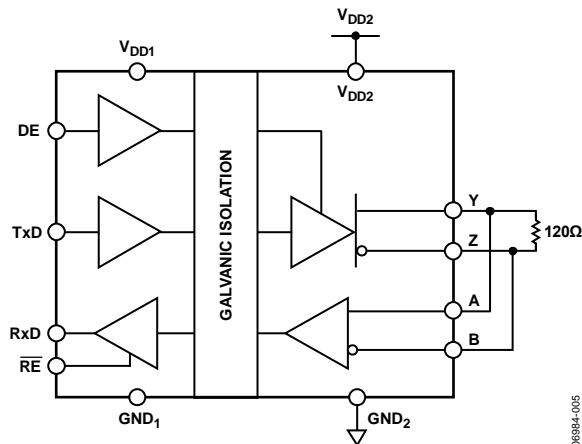


Figure 20. Supply Current Measurement Test Circuit

SWITCHING CHARACTERISTICS

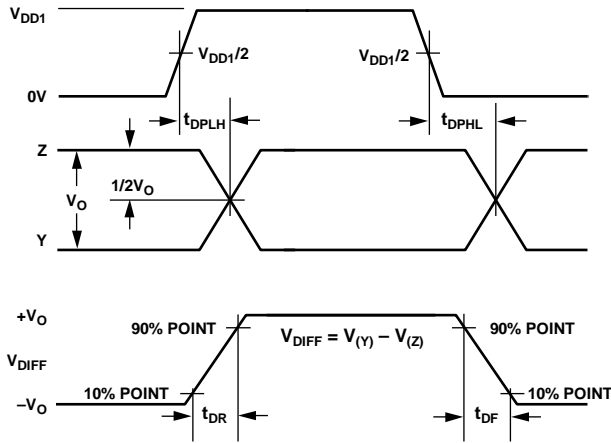


Figure 21. Driver Propagation Delay, Rise/Fall Timing

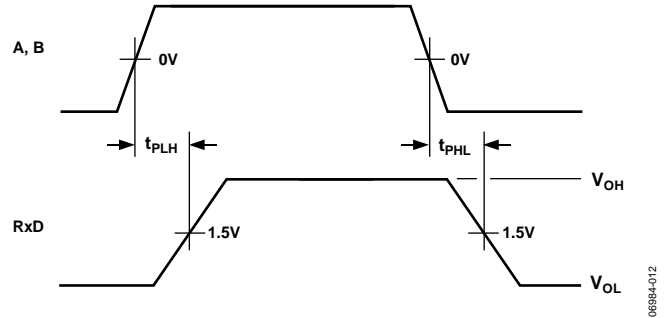


Figure 23. Receiver Propagation Delay

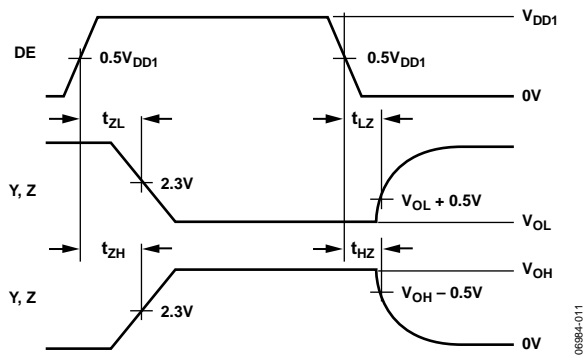


Figure 22. Driver Enable/Disable Delay

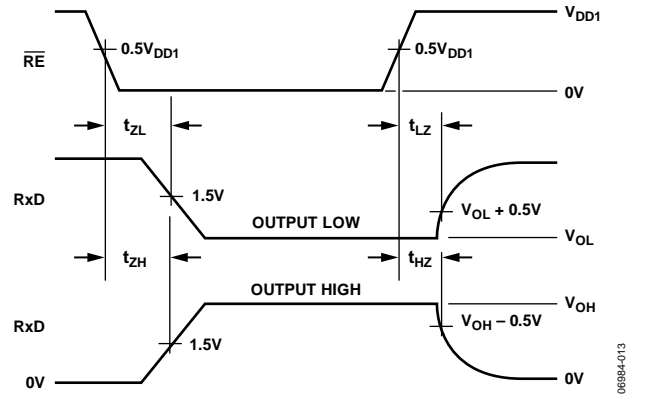


Figure 24. Receiver Enable/Disable Delay

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2484E, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 25). The driver input signal, which is applied to the TxD pin and referenced to the logic ground (GND₁), is coupled across an isolation barrier to appear at the transceiver section referenced to the isolated ground (GND₂). Similarly, the receiver input, which is referenced to the isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to the logic ground.

iCoupler Technology

The digital signals transmit across the isolation barrier using iCoupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the input cause narrow (approximately 1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than approximately 1 μs, a periodic set of refresh pulses, indicative of the correct input state, are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 μs, then the input side is assumed to be unpowered or nonfunctional, in which case the output is forced to a default state (see Table 11).

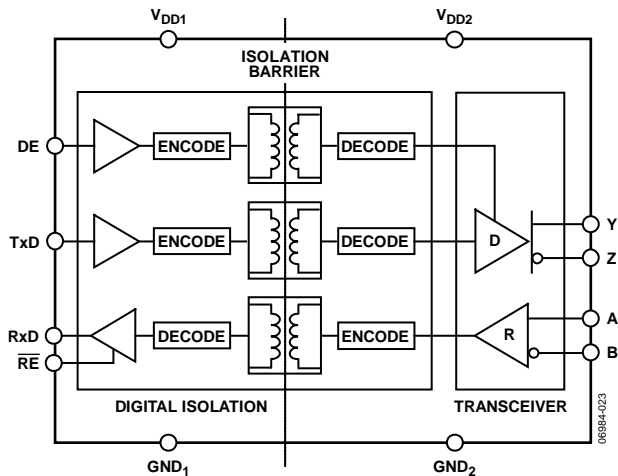


Figure 25. Digital Isolation and Transceiver Sections

TRUTH TABLES

The truth tables in this section use the abbreviations shown in Table 10.

Table 10. Truth Table Abbreviations

| Letter | Description |
|--------|----------------------|
| H | High level |
| L | Low level |
| I | Indeterminate |
| X | Irrelevant |
| Z | High impedance (off) |
| NC | Disconnected |

Table 11. Transmitting

| Supply Status | | Inputs | | Outputs | |
|------------------|------------------|--------|-----|---------|---|
| V _{DD1} | V _{DD2} | DE | TxD | Y | Z |
| On | On | H | H | H | L |
| On | On | H | L | L | H |
| On | On | L | X | Z | Z |
| On | Off | X | X | Z | Z |
| Off | On | L | X | Z | Z |
| Off | Off | X | X | Z | Z |

Table 12. Receiving

| Supply Status | | Inputs | | Output |
|------------------|------------------|----------------------|---------|--------|
| V _{DD1} | V _{DD2} | A – B (V) | RE | RxD |
| On | On | > -0.03 | L or NC | H |
| On | On | < -0.2 | L or NC | L |
| On | On | -0.2 < A – B < -0.03 | L or NC | I |
| On | On | Inputs open | L or NC | H |
| On | On | X | H | Z |
| On | Off | X | L or NC | H |
| Off | Off | X | L or NC | L |

THERMAL SHUTDOWN

The ADM2484E contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers re-enable at a temperature of 140°C.

TRUE FAIL-SAFE RECEIVER INPUTS

The receiver inputs have a true fail-safe feature ensuring that the receiver output is high when the inputs are open or shorted. During line-idle conditions, when no driver on the bus is enabled, the voltage across a terminating resistor at the receiver input decays to 0 V. With traditional transceivers, receiver input thresholds specified between -200 mV and +200 mV mean that external bias resistors are required on the A and B pins to ensure that the receiver outputs are in a known state. The true fail-safe receiver input feature eliminates the need for bias resistors by specifying the receiver input threshold between -30 mV and -200 mV. The guaranteed negative threshold means that when the voltage between A and B decays to 0 V; the receiver output is guaranteed to be high.

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the iCoupler is set by the condition in which an induced voltage in the receiving coil of the transformer is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADM2484E is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated.

The voltage induced across the receiving coil is given by

$$V = \left(\frac{-d\beta}{dt} \right) \sum \pi r_n^2 ; n = 1, 2, \dots, N$$

where:

β is the magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the n^{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field can be determined using Figure 26.

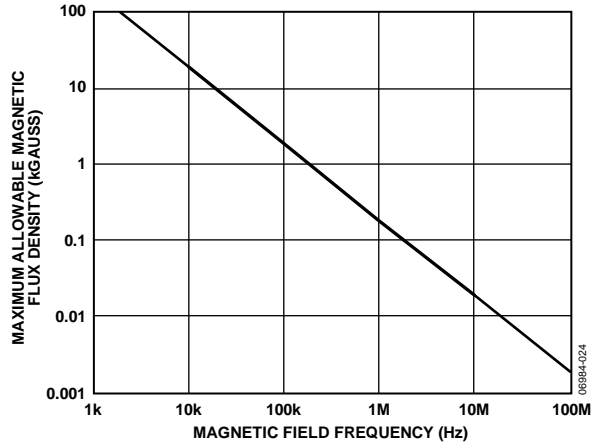


Figure 26. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

Figure 27 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow at given distances away from the ADM2484E transformers.

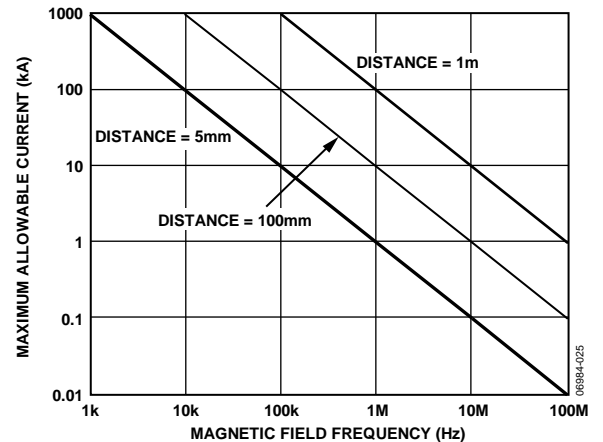


Figure 27. Maximum Allowable Current for Various Current-to-ADM2484E Spacings

With combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

ISOLATED POWER SUPPLY CIRCUIT

The ADM2484E requires isolated power capable of 3.3 V at up to approximately 75 mA (this current is dependent on the data rate and termination resistors used) to be supplied between the V_{DD2} and the GND₂ pins. A transformer driver circuit with a center tapped transformer and LDO can be used to generate the isolated 5 V supply, as shown in Figure 28. The center tapped transformer provides electrical isolation of the 5 V power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP3330 linear voltage regulator provides a regulated power supply to the bus-side circuitry (V_{DD2}) of the ADM2484E.

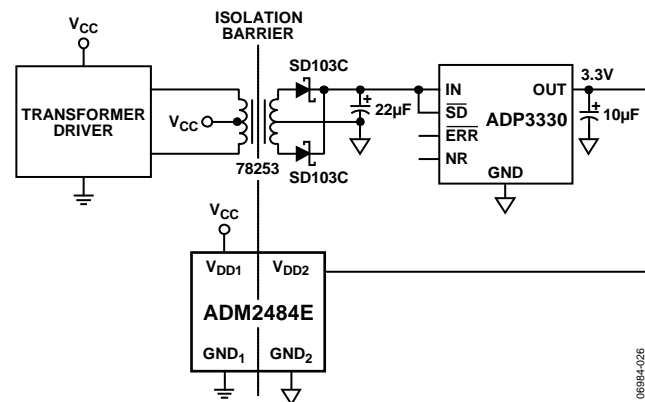


Figure 28. Isolated Power Supply Circuit

PC BOARD LAYOUT

The ADM2484E isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 29). Bypass capacitors are conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. Best practice suggests the following:

- A capacitor value between 0.01 µF and 0.1 µF.
- A total lead length between both ends of the capacitor and the input power supply pin that does not exceed 20 mm.
- Unless the ground pair on each package side is connected close to the package, consider bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16.

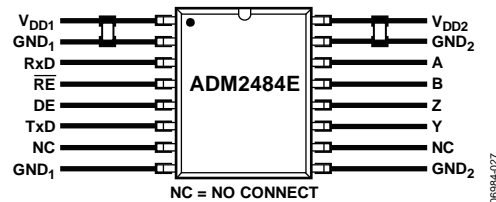


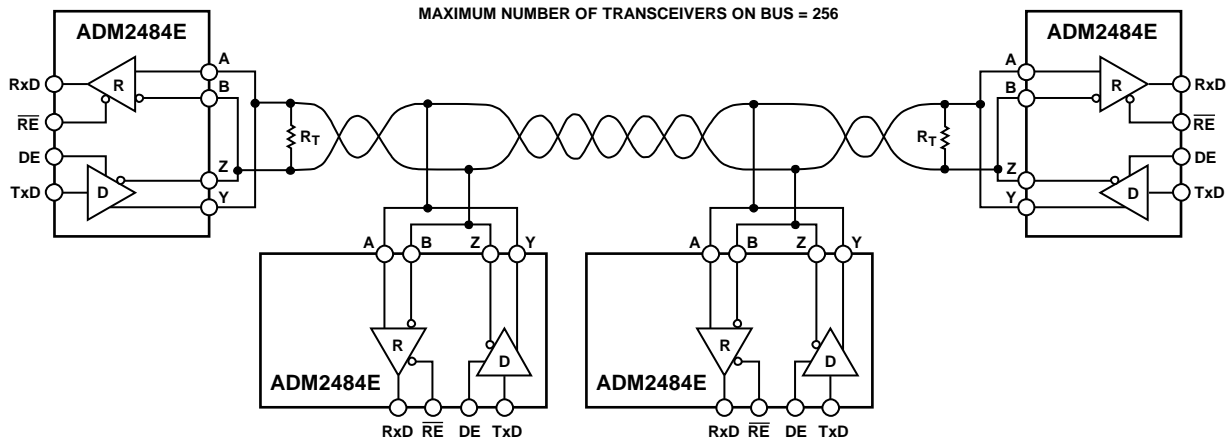
Figure 29. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

TYPICAL APPLICATIONS

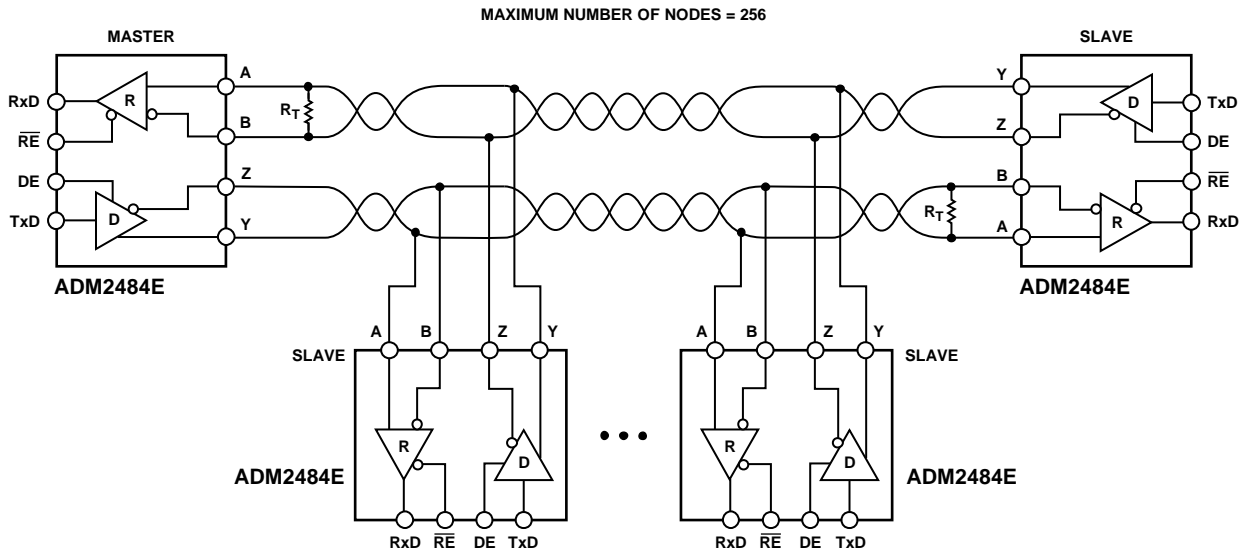
Figure 30 and Figure 31 show typical applications of the ADM2484E in half-duplex and full-duplex RS-485 network configurations. Up to 256 transceivers can be connected to the RS-485 bus. To minimize reflections, the line must be terminated

at the receiving end in its characteristic impedance, and stub lengths off the main line must be kept as short as possible. For half-duplex operation, this means that both ends of the line must be terminated, because either end can be the receiving end.



- NOTES
 1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.
 2. ISOLATION NOT SHOWN.

Figure 30. ADM2484E Typical Half-Duplex RS-485 Network



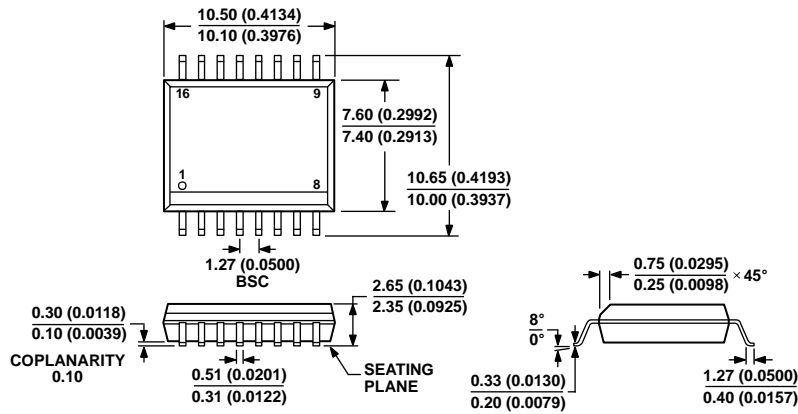
- NOTES
 1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

Figure 31. ADM2484E Typical Full Duplex RS-485 Network

06984-028

06984-029

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 32. 16-Lead Standard Small Outline Package [SOIC_W]
 Wide Body
 (RW-16)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|-------------------------------------------------|----------------|
| ADM2484EBRWZ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_W] | RW-16 |
| ADM2484EBRWZ-REEL7 | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_W] | RW-16 |
| EVAL-ADM2484EEBZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

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